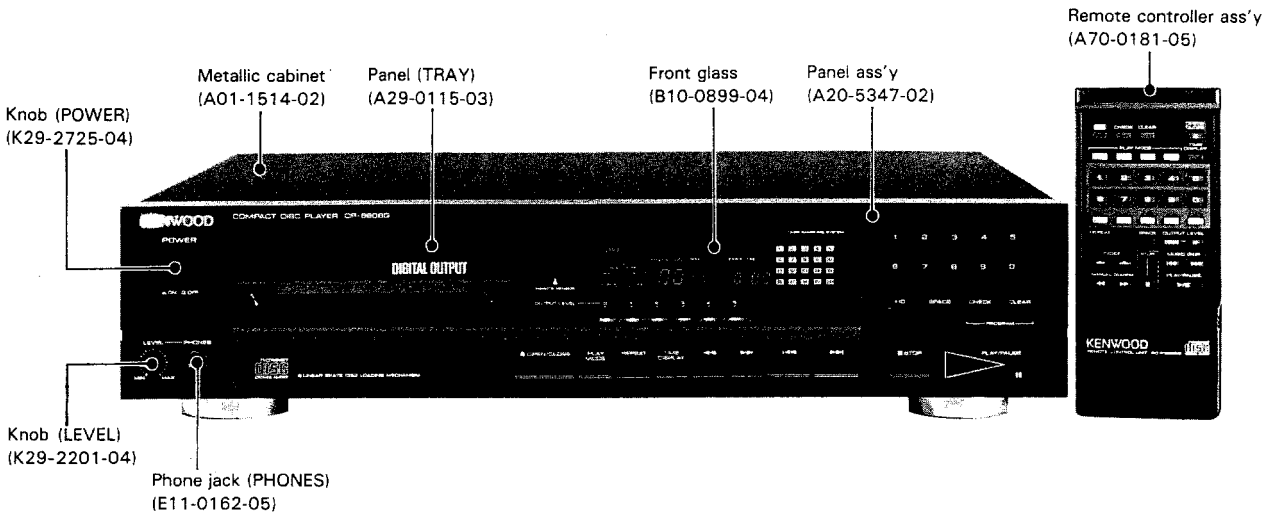
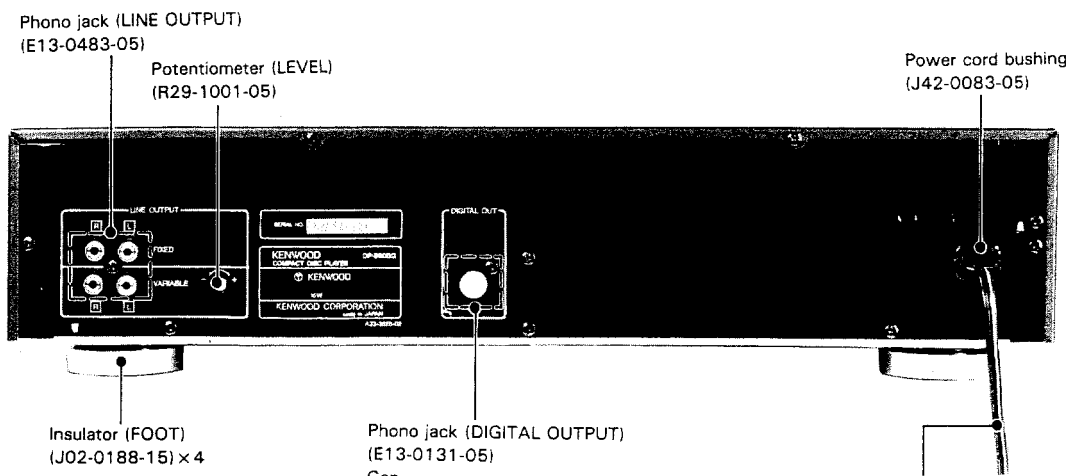
COMPACT DISC PLAYER

DP-880SG

SERVICE MANUAL

KENWOOD





In compliance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

KENWOOD Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040.10, Chapter I, Subchapter J.

DANGER: Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

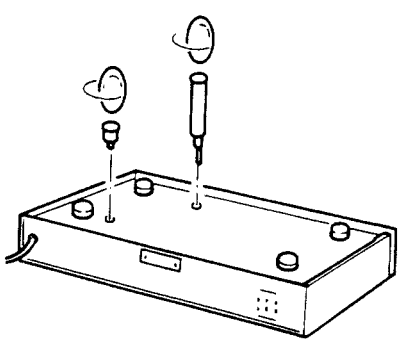
* Refer to parts list on page 81.

CONTENTS

TRANSPORTATION SCREW

Before operation, remove the two red screws attached to the bottom of the unit used during transport from the factory. Remove both screws using a coin, etc. and, after removing, retain them together with the Warranty card and other documents. When the unit is so be transported again, be sure replace the two screws to their original position:

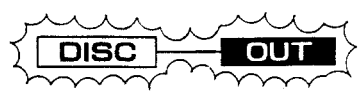
* For the procedure of attaching the transportation screws.



■ Before transport: tighten the transportation screws

Before transporting this unit, be sure to tighten the two transportation screws on the bottom of the unit.

1. Turn ON the power switch when no disc is loaded .
2. Wait a few seconds until the disc OUT indicator comes "ON". The turn "OFF" the power.

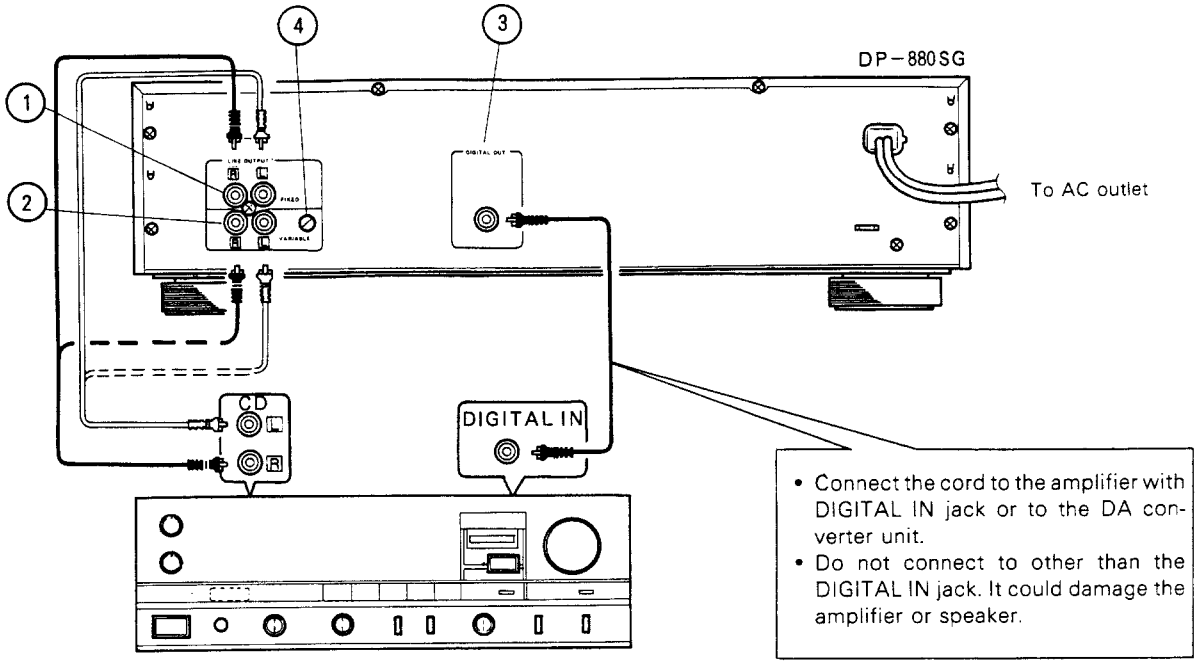


3. Firmly tighten the two transportation screws.

SYSTEM CONNECTIONS

Connection precautions

Always turn OFF the power before making connections.
Incorrect connections can cause damage to your audio system. Heed the precautions and follow the directions carefully.



- Connect the cord to the amplifier with DIGITAL IN jack or to the DA converter unit.
- Do not connect to other than the DIGITAL IN jack. It could damage the amplifier or speaker.

① **Fixed output (FIXED): Output voltage 2Vrms fixed**
Use these stereo output jacks for connection to a typical amplifier or receiver.

② **Variable output (VARIABLE): Output voltage 0~2Vrms variable**
You can adjust the output level from these jacks to match the signal level of other sources connected to your amplifier or receiver. (May also be used for adjusting recording level by remote control).

③ **Digital output (DIGITAL OUT) 0.5V p-p 75 ohms**

④ **Output level adjustment screw**
Turn this screw if you need to adjust output signal level for the variable output jacks. (You can see the result of adjustment on the front panel level indicators.)

■ Connection procedure

1. **Connection to amplifier or receiver**

- **Conventional amplifier connection:**
  Connect the CD player's LINE OUTPUT (FIXED or VARIABLE) to the AUX or CD input jacks on the rear panel of the amp or receiver. Use the supplied cord. Be sure to connect the left (L) and right (R) jacks on the CD player to the corresponding jacks on the amplifier or receiver.

- **Connection to an amplifier equipped with digital input:**
  Use a single coaxial cable to connect the CD player's DIGITAL OUT jack to the digital input jack on the amplifier.

2. **Plug in the AC power cord for the CD player and amplifier.**

❶ **POWER switch**

❷ **LEVEL control**
Adjusts headphone volume level

❸ **PHONES jack**
Plug stereo headphones into this jack.

❹ **OPEN/CLOSE key (⏏)**
Press once to open the disc tray. Press again to close.

❺ **PLAY MODE key**
The play mode changes each time you press this key. The mode sequence is:

TRACK → PROGRAM (PGM) → TIME → SINGLE

❻ **REPEAT key**
Used for repeated play.

❼ **TIME DISPLAY key**
This switches the time display.

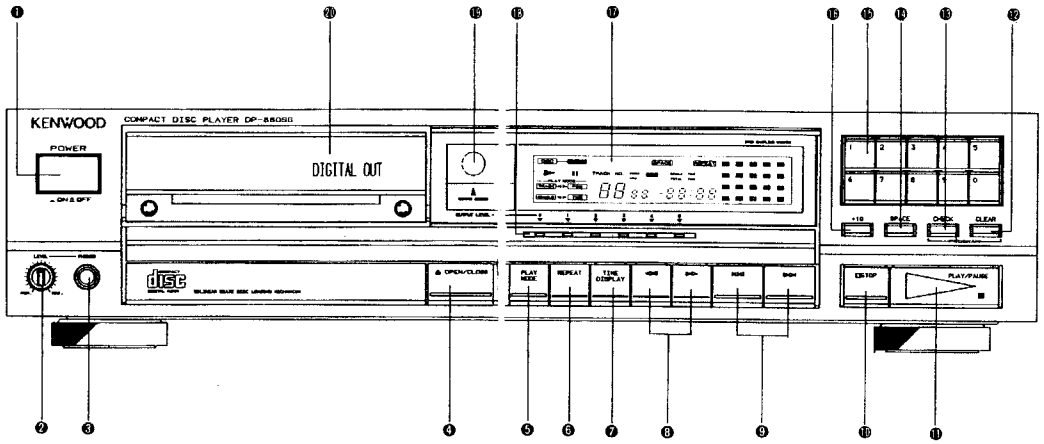
❽ **Manual search keys (◀◀ , ▶▶)**
These keys let you move quickly forward or backward across the disc.

❾ **Music skip keys (⏮ , ⏭)**
Used to skip forward to the start of the next selection or back to the start of the current or preceding selection.

❿ **STOP key (■)**
Press to stop play.

⓫ **PLAY/PAUSE key (▷/⏸)**
Press to begin play. Press during play to pause or resume play.

⓬ **CLEAR key**
This erases the last track in a program.



⓭ **CHECK key**
Press to check program contents.

⓮ **SPACE key**
This causes play to pause for about four seconds between tunes, useful when taping.

⓯ **Numeric keys (1 ~ 0)**
Used to specify first digit in a number when selecting a selection or setting a time.

⓰ **Plus ten key (+10)**
Adds ten to a number. Used with the numeric keys.

⓱ **DISPLAY**

⓲ **OUTPUT LEVEL indicator**
Six LEDs show the output level (of the signal from the VARIABLE jacks on the rear panel.) This can be adjusted by remote control or output level adjustment screw on the rearpanel.

⓳ **REMOTE SENSOR window**
This picks up infrared signals from the remote control.

⓴ **Disc tray**

Display Window

① **Play indicator (▶)**

② **PLAY MODE indicators**

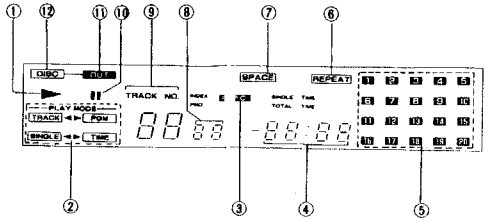
③ **Program check indicator (P.C.)**
Lights up when you check program contents.

④ **Time counter (TOTAL TIME, SINGLE TIME)**

⑤ **Music calendar (1 - 20)**
Indicates the track (selection) numbers on the disc, or shows which selections are programmed for play.

⑥ **REPEAT indicator**

⑦ **SPACE indicator**



⑧ **Index number (INDEX)/program number (P NO.)**
Shows the current index number within the track. Shows the number of tracks during programming or when checking program contents.

⑨ **Track number display (TRACK NO.)**
Shows the track number (according to the order of the selections on the disc).

⑩ **Pause indicator (⏸)**

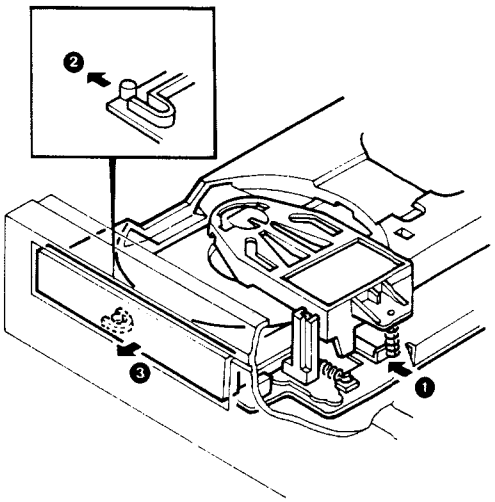
⑪ **Disc out indicator (OUT)**
This illuminates (red) when there is no disc in the tray.

⑫ **Disc indicator**
Confirms that a disc is in the tray.

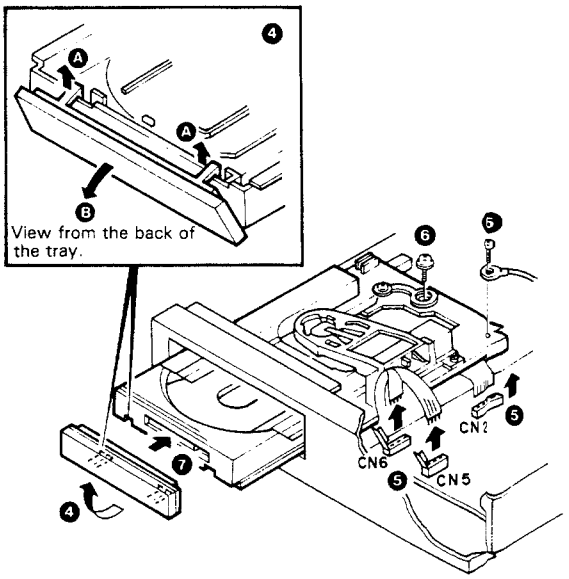
DISASSEMBLY FOR REPAIR

1. Mechanism assembly removal procedure

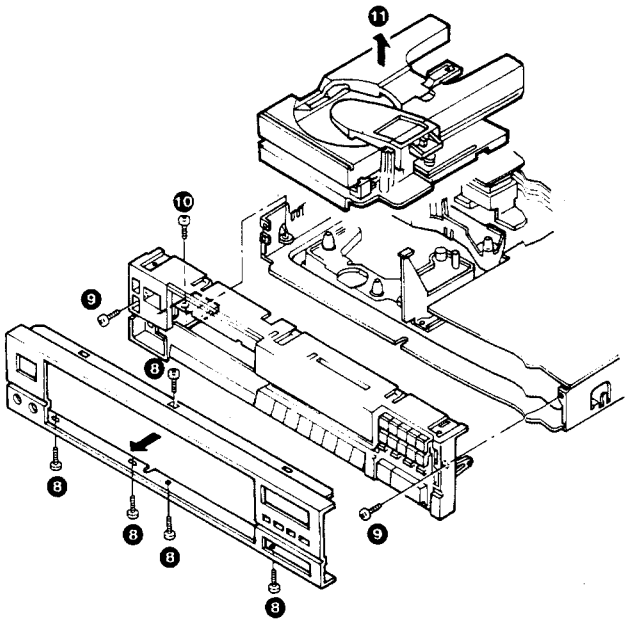
1. Push the protrusion of the slider ass'y located on the bottom of the disc clamper in the direction of the arrow (❶).
2. The roller of the slider ass'y can be removed from the stop position (❷).
3. Remove the tray by pulling out gently in the direction of the arrow (❸).



4. Release the two claws of the tray panel by lifting up gently in the direction of the arrow (Ⓐ), and take it off in the direction of the arrow (Ⓑ). (❹)
5. Remove the two wire clampers, the flexible printed board (❺), mechanism retaining screw (❻) and the ground lug retaining screw (❻) from the mechanism.
6. Push the tray in again in the direction of the arrow (❼).



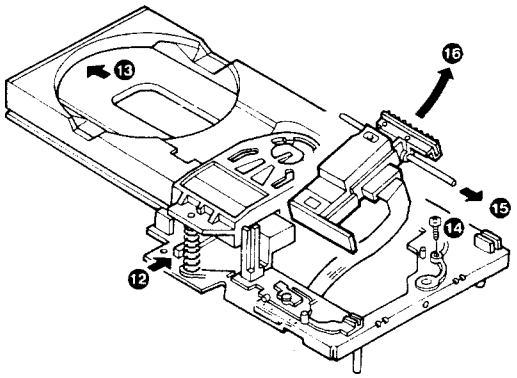
7. Remove the five screws (❽) retaining the front panel, and take out the front panel.
8. Remove the two screws (❾) retaining the sub panel, and the screw (❿) retaining the PHONES PC board.
9. Remove the mechanism assembly in the direction of the arrow (⓫).



DISASSEMBLY FOR REPAIR

2. Pickup removal procedure

1. Push the protrusion of the slider main assembly located on the bottom of the disc clamper in the direction of the arrow (⓬).
2. While pressing it in the direction of the arrow (⓬), remove the tray by pulling out in the direction of the arrow (⓭).
3. Remove the pickup rail retaining screw (⓮).
4. Slide the laser pickup in the direction of the arrow (⓯), and pull it out gently in the direction of the arrow (⓰).



Note: Since the flexible PC board from the laser pickup is partly fixed to the mechanism chassis, do not pull it out forcibly. When reassembling the laser pickup, secure the flexible PC board to the fixing hook of the mechanism assembly firmly.

CIRCUIT DESCRIPTION

Description of components

Electric Unit (X25-312X-XX)

Component	Use/function	Operation/condition/compatibility
IC1 NJM4558D	Op amp	Digital ±5 V constant power supply error amplifier
IC2 M5218P	Op amp	Analog ±12 V constant power supply error amplifier
IC3 M5218P	Op amp	Analog ±5.5 V constant power supply error amplifier
IC4 M5218P	Op amp	Analog ±5 V constant power supply error amplifier
IC5 NJM4558D	Op amp	(1/2) For remote volume drive. (UP: +5 V, DOWN: −5 V) (2/2) For reset circuit. Output high level signal when digital +4.4 V or less signal is received.
IC6 NJM4558D	Op amp	IC for headphones
IC7, 8 NJM4560	Op amp	IC for line amp. LPF (sampling pulse elimination)
IC9 NJM4558D	Op amp	(1/2) PLL compensation circuit (LPF+amp) (2/2) CLV compensation circuit (LPF+level shifter)
IC10, 11 PCM56P-K	D/A converter	Resistance ladder type D/A converter; Converts digital data into the volume of analog data.
IC12 TC17G005AF-0048	D/A distortion compensation	D/A distortion compensation
IC13 CXD1088Q	Digital filter	4 times oversampling digital filter
IC14 CXD1125QZ	Digital signal processing LSI	EFM data decoding, correction, interpolation, PLL circuit. All digital signal processing, including CLV servo, digital output, are performed in here.
IC15 CXK5816SP	Static RAM	Signal processing RAM (16 K)
IC16 μPD75208CW-152	Microprocessor	Input processing for display and each key input. Servo IC control.
IC17 CXA1081S	RF amp	Focus error signal generation and tracking error signal generation. RF signal generation and phase compensation.
IC18 μPD4053BC	Defect	Focus, tracking and feed control
IC19 CXA1244S	Servo IC	Each pulse signal generator for focus servo, tracking servo and feed servo. (Shrink type of CX202108)
IC20 LA6500	Driver	Voltage/current amplifier for focus coil
IC22 TC74HC02P	NAND gate	Digital out signal drive.
IC23 NJM4558D	Op amp	Current booster for tracking coil, feed motor and tray motor.
IC25 STA341M	Driver	voltage/current amplifier for tracking coil, feed motor and tray motor.
Q1 2SB772 (Q, P)	Ripple filter	Ripple filter for digital +5 V constant power supply.
Q2 2SD882 (Q, P)	Ripple filter	Ripple filter for digital −5 V constant power supply
Q3 2SD1266 (Q, P)	Ripple filter	Ripple filter for analog +12 V constant power supply
Q4 2SB941 (Q, P)	Ripple filter	Ripple filter for analog −12 V constant power supply
Q5 DTC124EN	Switch	For discharging of reset condenser C28.
Q6 2SC3666 (Y)	Driver	VARIABLE volume motor driver
Q7 2SA1426 (Y)	Driver	VARIABLE volume motor driver
Q8 2SA1284 (Q, P)	Ripple filter	For −24 V constant power supply control for FL display
Q9 2SA999 (E, F)	Ripple filter	For −24 V constant power supply error amp for FL display
Q10 DTA124EN	Switch	Deemphasis control switch
Q11 DTC124EN	Switch	Deemphasis control switch
Q12 2SC2320 (E, F)	Driver	Muting relay driver
Q13, 14 2SC2878	Switch	Deemphasis switch
Q15, 16 2SA954 (L, K)	Driver	Headphone amp driver
Q17, 18 2SC2003 (L, K)	Driver	Headphone amp driver
Q19 2SD882 (Q, P)	Driver	Disc motor driver
Q20 2SA1534A	Driver	Disc motor driver
Q21 2SA999 (E, F)	Driver	Current booster for FL display
Q22 DTC124EN	Driver	Current booster for FL display

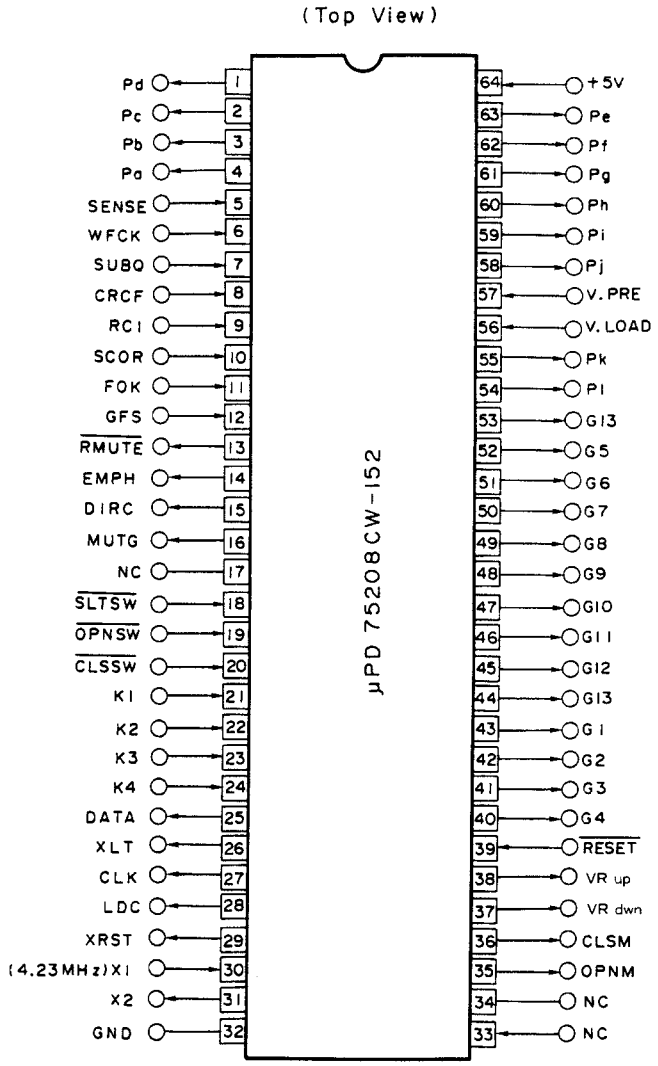
CIRCUIT DESCRIPTION

Operation unit (X25-313X-XX)

Component	Use/function	Operation/condition/compatibility
IC1 LB1433N	Level meter circuit	Level display for remote volume control
IC2 GP-1U501	Remote control signal receiving device	Converts the signal from the infrared remote control unit into logic level signal

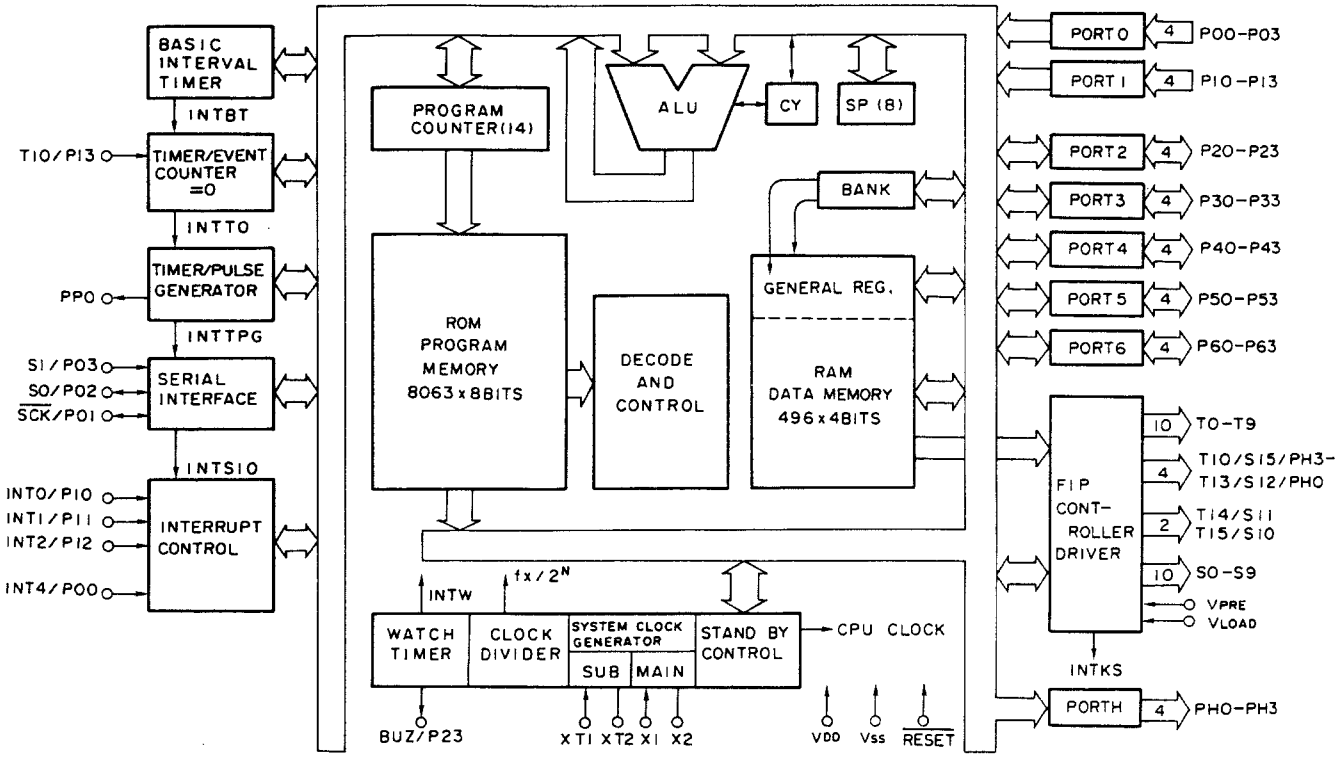
Semiconductor data

IC16: μPD75208CW-152 (X25-3120-11)
Microprocessor



CIRCUIT DESCRIPTION

Block diagram



Pin description

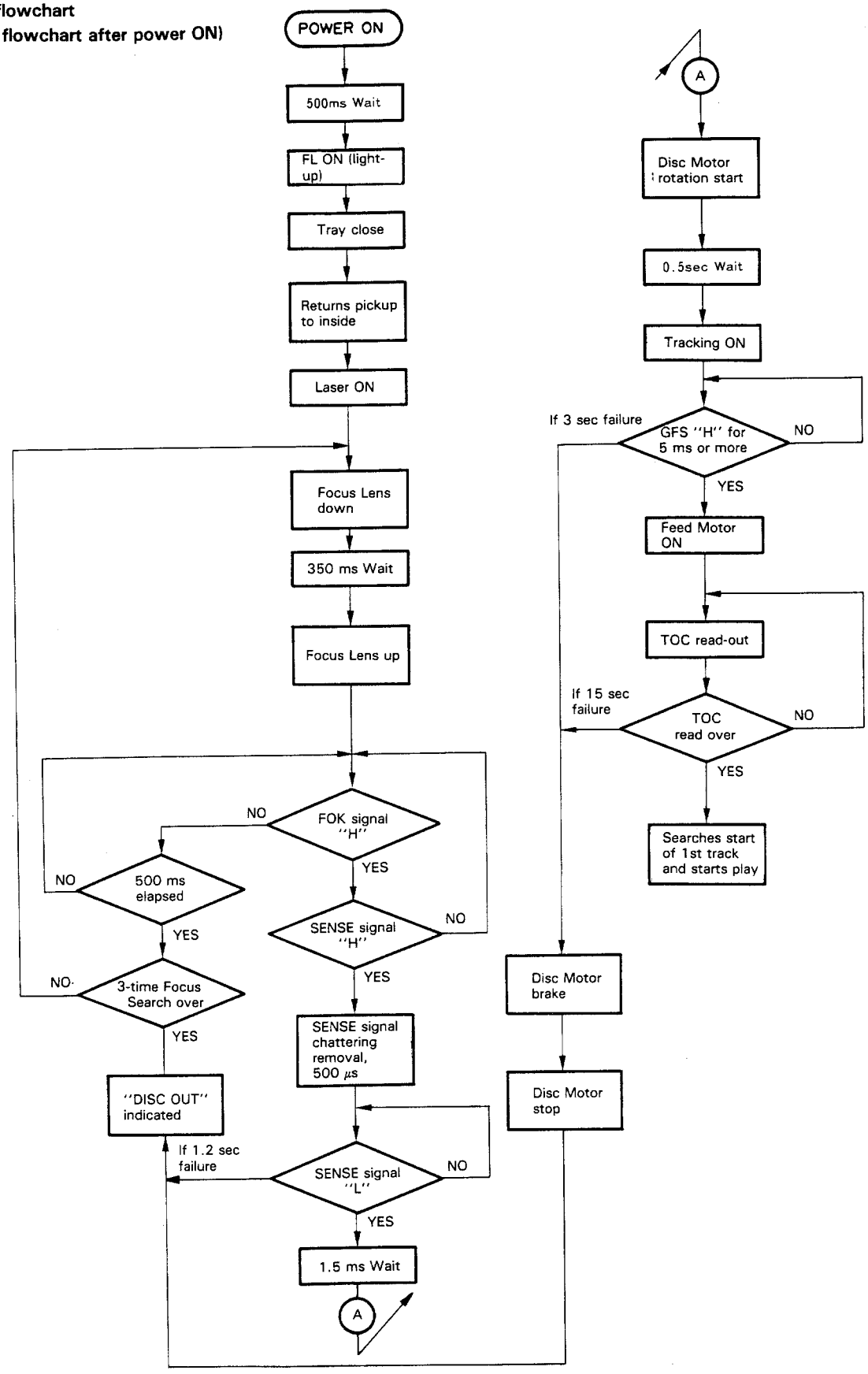
Pin No.	Symbol	I/O	Pin name	Functions
1	S3	O	Pd	FL display segment indication and key scan signal output
2	S2	O	Pc	
3	S1	O	Pb	
4	S0	O	Pa	
5	P00/INT4	I	SENSE	Sensing signal input (from CXD1125, CXA1244)
6	P01/$\overline{SCK}$	I	WFCK	Q data read-off clock input (from CXD1125)
7	P02/SO	I	SUBQ	Q data input (from CXD1125)
8	P03/SI	I	CRCF	Q data CRC OK ("H") input (from CXD1125)
9	P10/INT0	I	RCI	Remote control signal input
10	P11/INT1	I	SCOR	Q data sync signal input (from CXD1125)
11	P12/INT2	I	FOK	Focus OK ("H") input (from CXD1088Q)
12	P13/TI0	I	GFS	EFM sync OK ("H") input (from CXD1125)
13	P20	O	$\overline{RMUTE}$	Relay mute ON/OFF ("L"/"H")
14	P21	O	EMPH	Emphasis ON/OFF ("H"/"L")
15	P22	O	DIRC	DIRC signal output (to CXA1244)
16	P23	O	MUTG	MUTG signal output; Mute ON/OFF ("H"/"L") (to CXD1125)
18	P31	I	$\overline{SLT\ SW}$	Start limit switch signal input (SW ON = "L")
19	P32	I	$\overline{OPN\ SW}$	Tray open switch signal input (SW ON = "L")
20	P33	I	$\overline{CLS\ SW}$	Tray close switch signal input (SW ON = "L")
21	P60	I	K1	Key input for front panel
22	P61	I	K2	
23	P62	I	K3	
24	P63	I	K4	

CIRCUIT DESCRIPTION

Pin No.	Symbol	I/O	Pin name	Functions
25	P40	O	DATA	Control data signal output (to CXD1125, CXA1244)
26	P41	O	XLT	Control data latch signal output (to CXD1125, CXA1244)
27	P42	O	CLK	Control data clock signal output (to CXD1125, CXA1244)
28	P43	O	LDC	Laser ON/OFF ("H"/"L") signal output
29	PPO	O	XRST	Control reset signal output (to CXD1125, CXA1244)
30	X1	I	X1	Clock input pin (1/2 clock of CXD1125) (Oscillating frequency 4.2336 MHz)
31	X2	O	X2	
32	Vss	—	Vss	GND
35	P50	O	OPNM	Tray open/close signal output Normal (OPNM = "L", CLSM = "L") Open (OPNM = "H", CLSM = "L") Close (OPNM = "L", CLSM = "H")
36	P51	O	CLSM	
37	P52	O	VRDWN	Motor volume level down signal output
38	P53	O	VRUP	Motor volume level up signal output
39	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$	Reset signal input
40 ≀ 53	T0 ≀ T13	O	G1 ≀ G13	FL display digit indication output T0—G4 T4—G13 T8—G9 T12—G5 T1—G3 T5—G12 T9—G8 T13—G13 T2—G2 T6—G11 T10—G7 T3—G1 T7—G10 T11—G6
54	T14/S11	O	PI	FL display segment indication output
55	T15/S10	O	Pk	
56	VLOAD	I	VLOAD	Negative power supply for FL display driver (−34 V)
57	VPRE	I	VPRE	Negative power supply for FL display predriver (−5 V)
58 ≀ 63	S9 ≀ S4	O	Pj ≀ Pe	FL display segment indication and key scan signal output
64	VDD	I	VDD	+5 V power supply

CIRCUIT DESCRIPTION

Set mode flowchart
(Simplified flowchart after power ON)

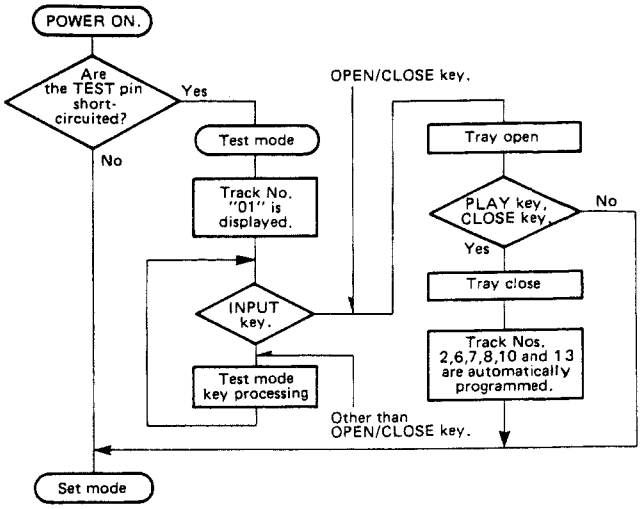


CIRCUIT DESCRIPTION

Test mode

In the DP-880SG, by short-circuiting between pin 7 and pin 8 of the electrical section unit (X25-3120-11), this microcomputer can be set to the test mode.

Note: "Set mode" shows the normal status.



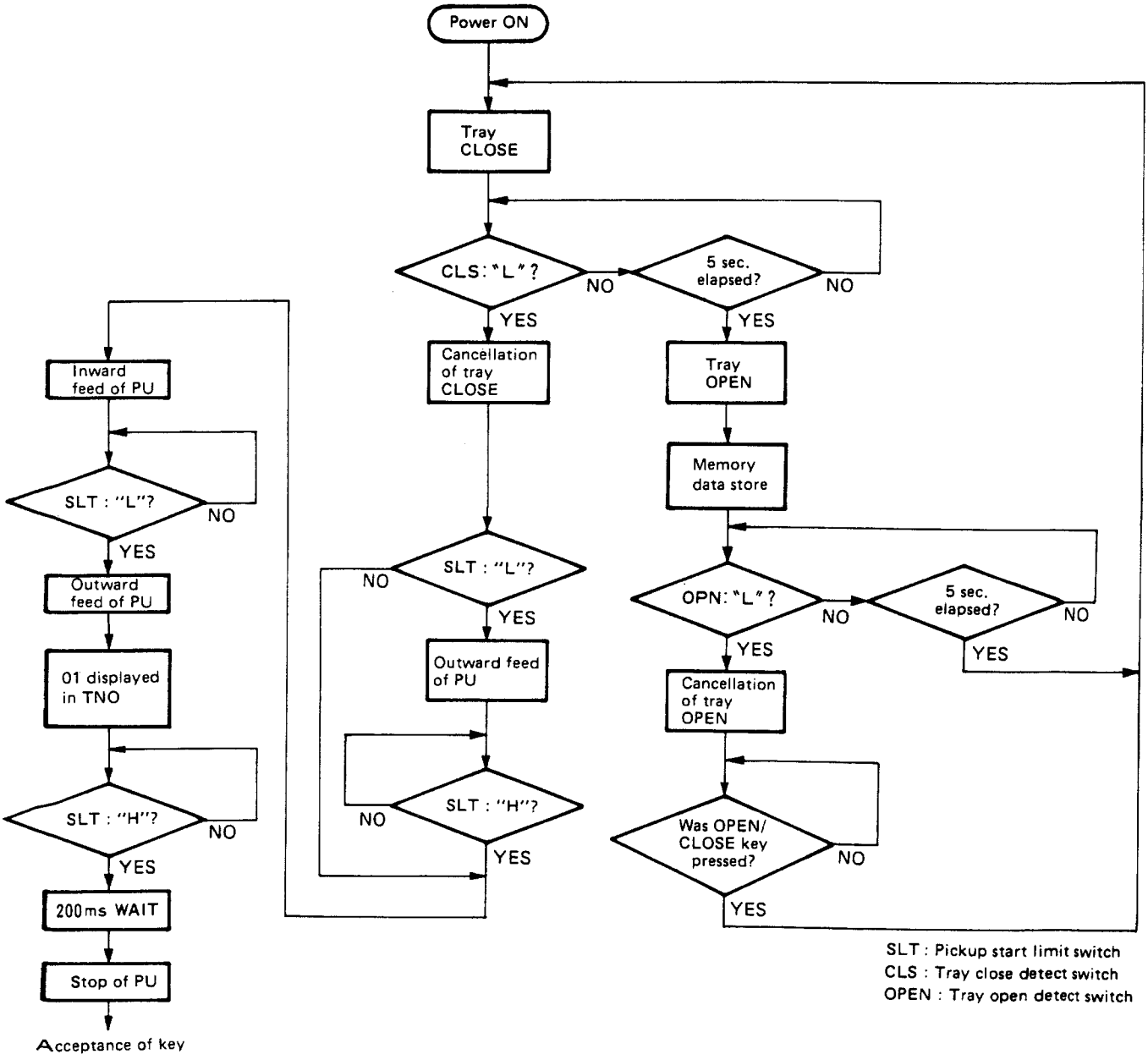
- **Effective keys in the Test mode and their functions**

No.	Input key	Function	Track No. display
1	PLAY	(1) Focus servo ..... ON. (2) Tracking servo..... ON. (3) Feed servo..... ON. When the key is pressed in the Stop mode, the servoes are switched ON automatically in the order from (1) to (3).	TRACK NO. 05 ↓ Displayed for a few seconds after (1) to (3). ↓ Disc's Track No. is displayed.
2	CHECK	(1) Focus servo ..... ON. (2) Tracking servo..... OFF. (3) Feed servo..... OFF.	TRACK NO. 03
3	CLEAR	(1) Focus servo ..... ON. (2) Tracking servo..... ON. (3) Feed servo..... OFF.	TRACK NO. 04
4	STOP	(1) Focus servo ..... OFF. (2) Tracking servo..... OFF. (3) Feed servo..... OFF.	TRACK NO. 01
7	+10	(1) Tray open (2) Laser..... ON. When the tray is closed by pressing it, +10 function will be released. The TRACK NO. display shows "01".	TRACK NO. 02
8	OPEN/CLOSE	When the tray is opened and the closed again in test mode, TRACK NOs. 2, 6, 7, 8, 10, 13 and 22 are automatically programmed. Opening the tray again will cause the unit to enter set mode.	

CIRCUIT DESCRIPTION

Flow chart of test mode

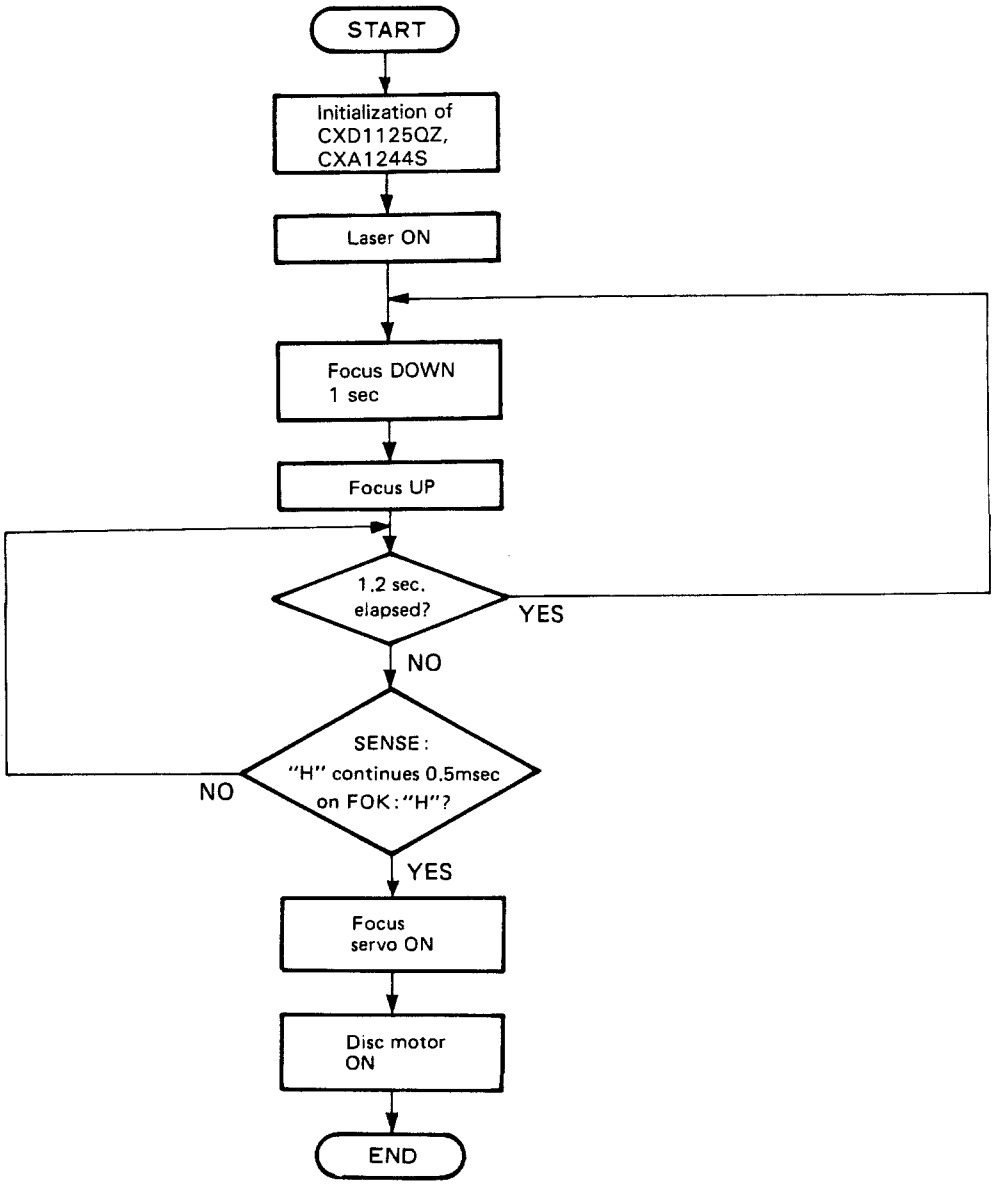
- **Flow chart from tray OPEN status after power ON**



SLT : Pickup start limit switch
CLS : Tray close detect switch
OPEN : Tray open detect switch

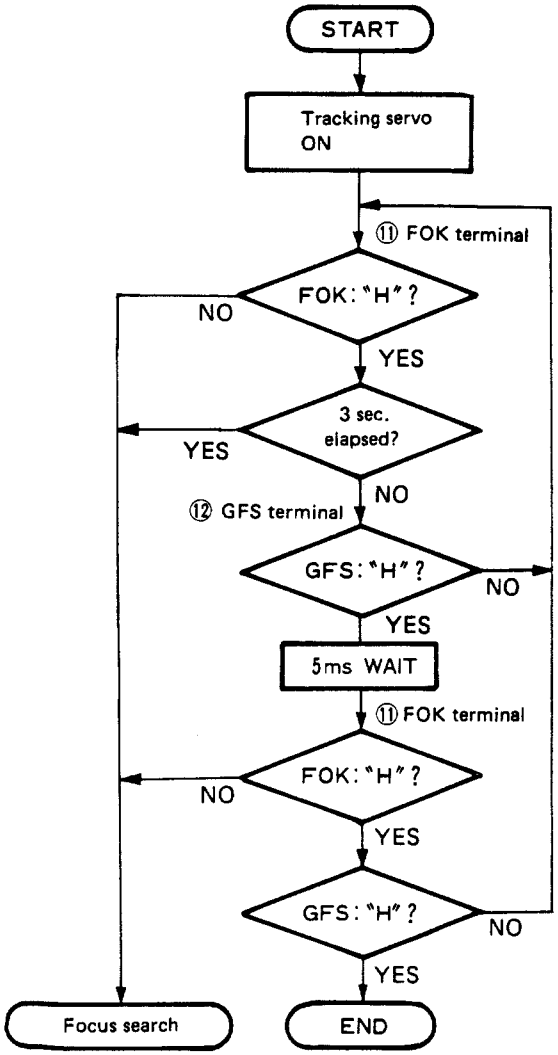
CIRCUIT DESCRIPTION

- **Focus search & focus servo ON**

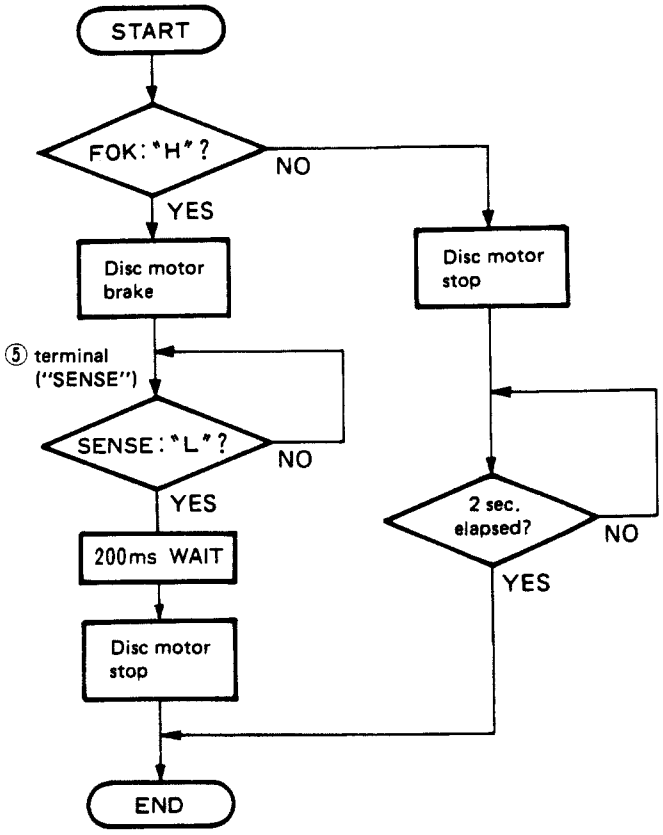


CIRCUIT DESCRIPTION

- **Tracking servo ON**

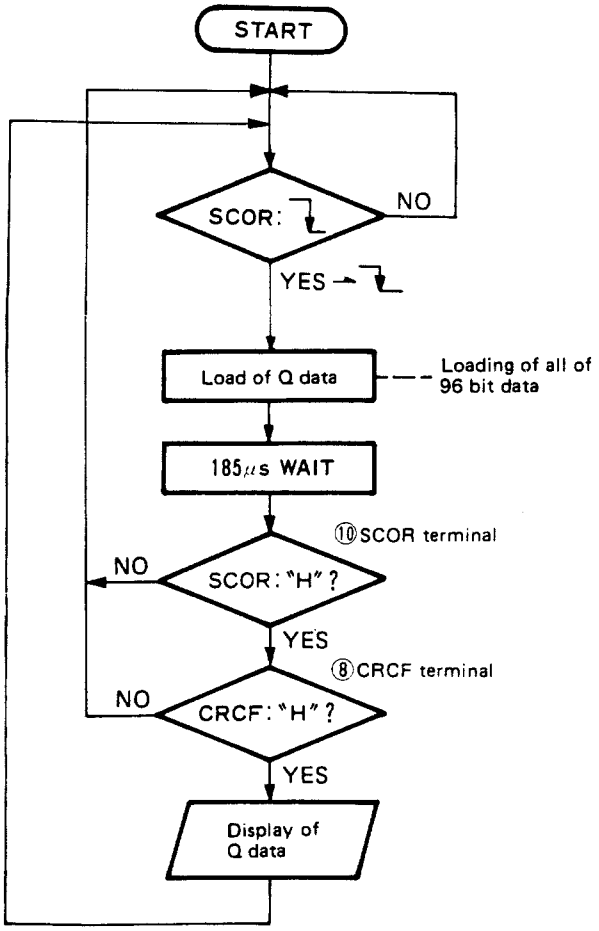


- **Disc motor stop**

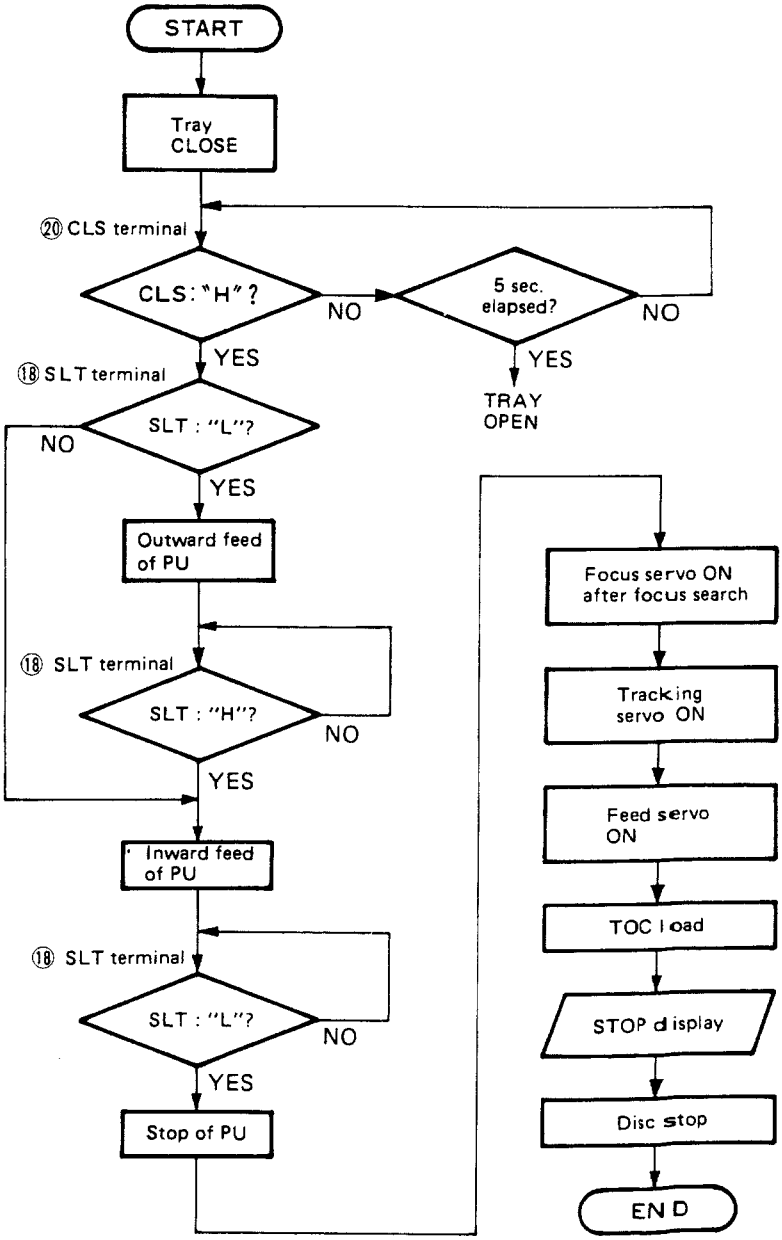


CIRCUIT DESCRIPTION

- **From loading of Q data to display**



- **Flow chart from the time the tray opens until the STOP indicator lights, after pressing the tray.**



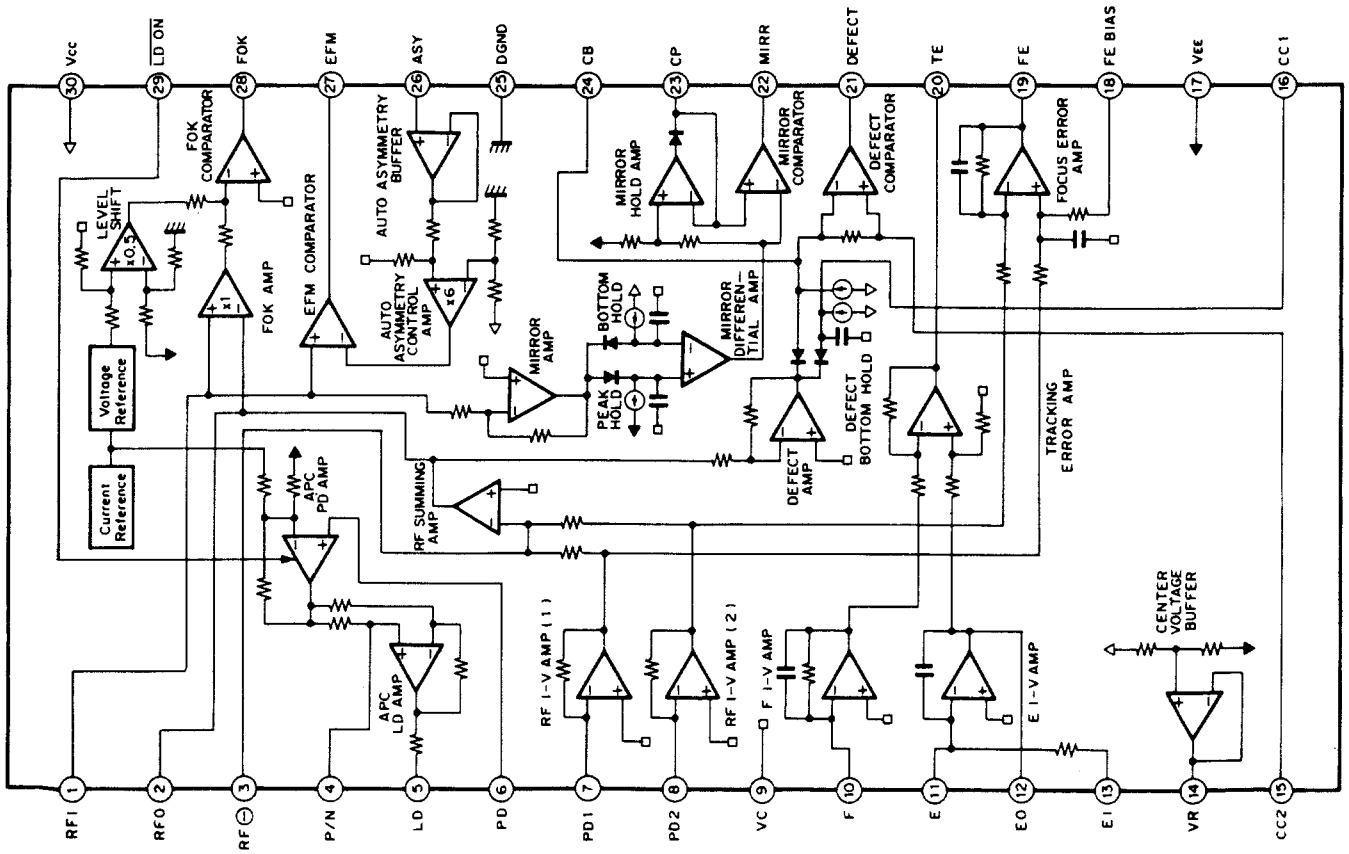
CIRCUIT DESCRIPTION

IC17: CXA1081S (X25-3120-11)
RF amplifier

The CXA1081S supplies the following functions as required for controlling the RF amp in the compact disc player.

- RF amp
- Focusing error amp
- Tracking error amp
- APC circuit
- Auto asymmetry control amp
- Focus OK detection circuit
- Mirror detection circuit
- Defect detection circuit
- EFM comparator

Block diagram



CIRCUIT DESCRIPTION

Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	RFI	I	Input pin of the C-coupled signal output from the RF summing amp.
2	RFO	O	Check point of eye pattern for the RF summing amp output pin.
3	RF ⊖	I	RF summing amp feedback input pin.
4	P/N	I	P-sub/L-sub select pin of LD. (DC voltage: in N-sub mode)
5	LD	O	APC LD amp output pin. (DC voltage: PD open in N-sub mode)
6	PD	I	APC PD amp input pin. (DC voltage: open)
7	PD1	I	RF I–V amp (1) invert input pin. Current input by connecting to PIN diode A + C.
8	PD2	I	RF I–V amp (2) invert input pin. Current input by connecting to PIN diode B + D.
9	VC	–	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
10	F	I	F I–V amp invert input pin. Current input by connecting to PIN diode F.
11	E	I	E I–V amp invert input pin. Current input by connecting to PIN diode E.
12	EO	O	E I–V amp output pin.
13	EI	I	E I–V amp feedback input pin. For E I–V amp gain adjustment.
14	VR	O	DC voltage output pin of (Vcc + VEE)/2.
15	CC2	I	Input pin of the C-coupled signal output from the defect bottom hold.
16	CC1	O	Defect bottom hold output pin.
17	VEE	–	Connected to the negative power supply when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
18	FE BIAS	I	Bias pin at the focus error amp non-invert side. For CMR adjustment of the focus error amp.
19	FE	O	Focus error amp output pin.
20	TE	O	Tracking error amp output pin.
21	DEFECT	O	Defect comparator output pin. (DC voltage: connected to a 10kΩ load).
22	MIRR	O	Mirror comparator output pin. (DC voltage: connected to a 10kΩ load).
23	CP	I	Mirror hold capacitor output pin. Mirror comparator non-invert input.
24	CB	I	Defect bottom hold capacitor connect pin.
25	DGND	–	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND (VEE) when using a single-voltage power supply.
26	ASY	I	Auto asymmetry control input pin.
27	EFM	O	EFM comparator output pin. (DC voltage: connected to a 10kΩ load).
28	FOK	O	FOK comparator output pin. (DC voltage: connected to a 10kΩ load).
29	$\overline{\text{LD ON}}$	I	LD ON/OFF select pin. (DC voltage: when LD ON).
30	Vcc	–	Positive power supply.

CIRCUIT DESCRIPTION

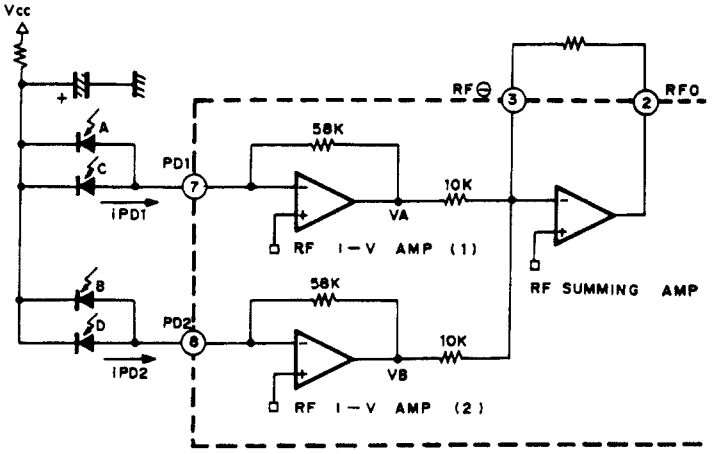
Explanation of function

- **RF amp**

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58kΩ in RF I–V amp (1) and (2) respectively. The voltage which is converted from the current of the photodiode (A + B + C + D) is added in the RF summing amp and is output from the RFO pin. The eye pattern can be checked at this pin.

The low frequency component of the RFO output voltage, V_{RFO} is represented by the following equation:

$$V_{RFO} = 2.2 \times (V_A + V_B)$$
$$= 127.6k\,\Omega \times (i_{PD1} + i_{PD2})$$



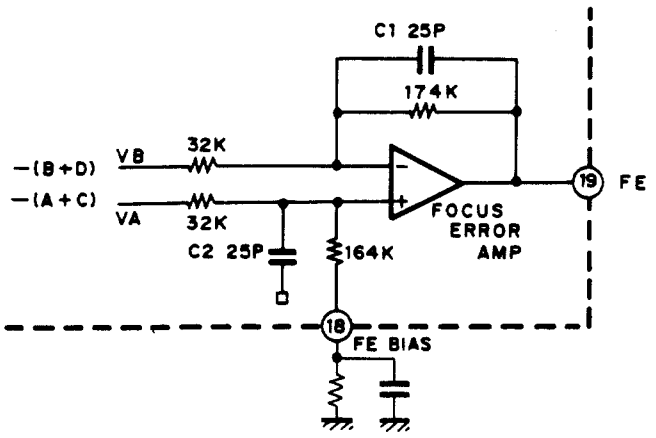
RF I–V amplifier

- **Focus error amp**

The difference between the RF I–V amp (1) output (VA) and the RF I–V amp (2) output (VB) is calculated, and the current of the photodiode (A + C – B – D) is converted to a voltage and output.

The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (i_{PD2} - i_{PD1}) \times 315.4k\,\Omega$$



CIRCUIT DESCRIPTION

- **Tracking error amp**

The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I–V amp and F I–V amp respectively. That is:

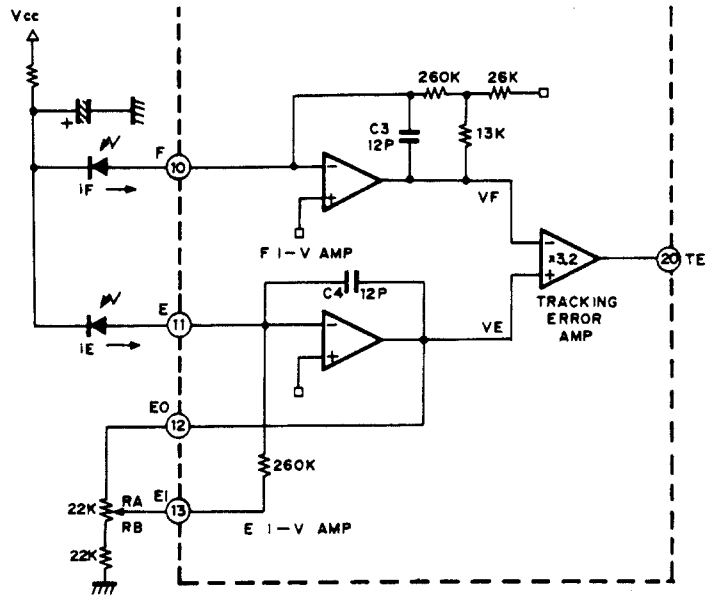
$$V_F = iF \times 403k\,\Omega$$

$$V_E = iE \times 260k\,\Omega \times R_A/(R_B + 22k) + (R_A + 260k)$$

The difference between the E I–V amp and the F I–V amp is calculated by the tracking error amp, and the photodiode (E–F) current is converted to a voltage and output.

$$V_{TE} = (V_E - V_F) \times 3.2$$

$$= (iE - iF) \times 1290k\,\Omega$$



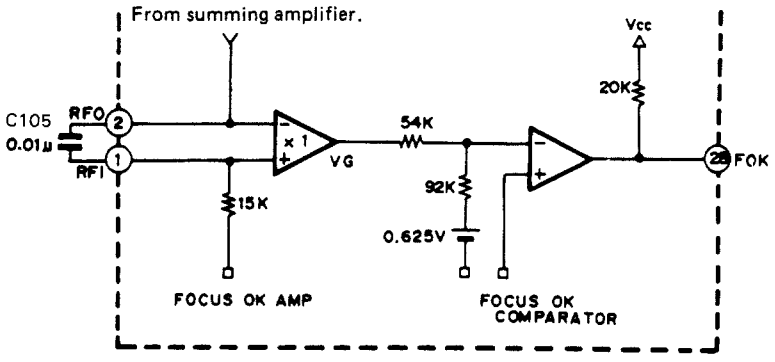
- **Focus OK circuit**

The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.

While the RF signal is present at pin 2, its HPF output is present at pin 1. At the same time, the LPF output (opposite phase) of the focus OK amp is obtained.

The focus OK output is inverted when $V_{RFI} - V_{RFO} \fallingdotseq -0.37V$.

C105 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amp. Normally, C105 = 0.01μF is selected, with fc = 1kHz. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.



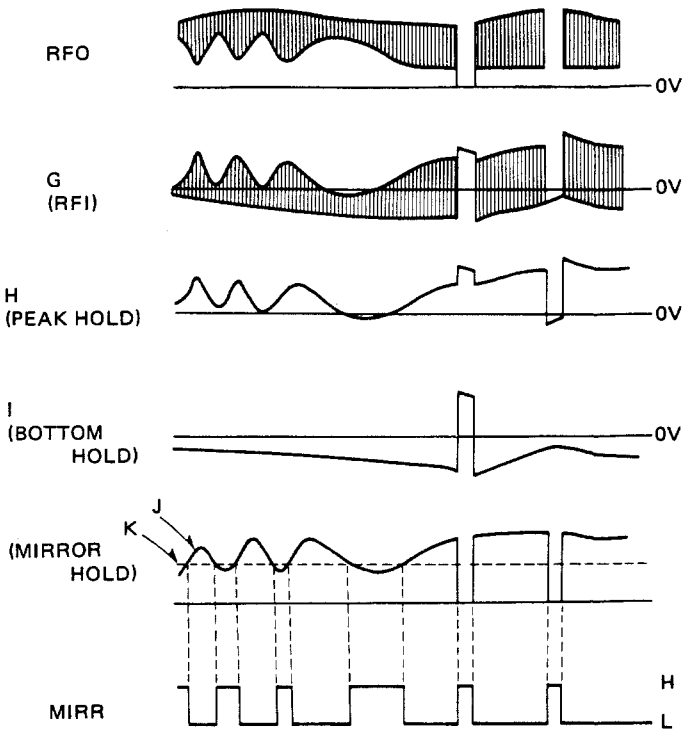
CIRCUIT DESCRIPTION

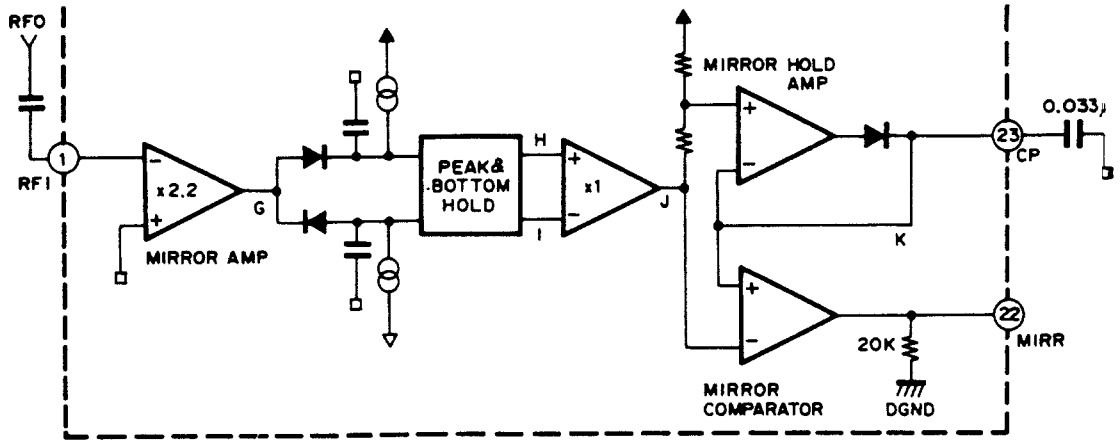
- **Mirror circuit**

In the mirror circuit, after the RFI signal is amplified, both peak and bottom holds are held by a time constant which can follow a traverse of 30kHz, while only the bottom hold is held by a time constant which can follow a cyclic period envelope variation respectively.

These peak/bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J.

This signal is compared with signal K, that the 2/3 level of the peak value is peak held by a large time constant so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite larger when compared with the traverse signal.





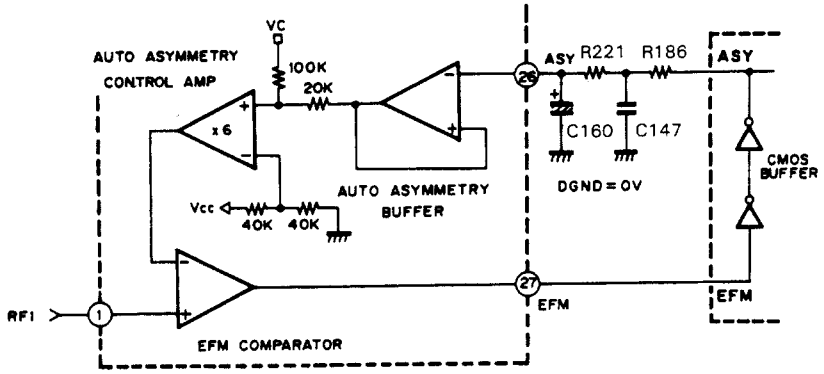
CIRCUIT DESCRIPTION

- **EFM comparator**

The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristics that the present probability of a 1 or 0 is 50% each for the binary coded EFM signal.

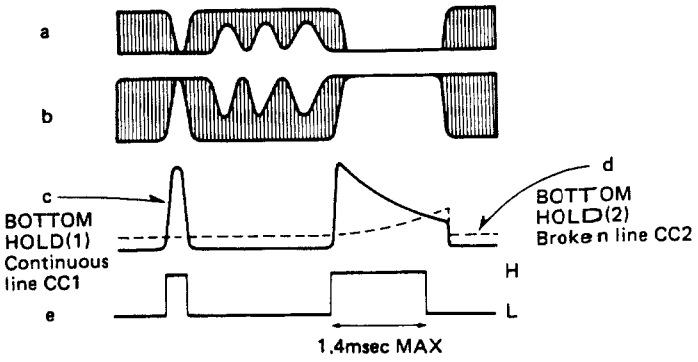
The EFM comparator is designed as a current switching type, and the "H" and "L" levels are not equal to the power voltages. Therefore, feedback is required via a CMOS buffer.

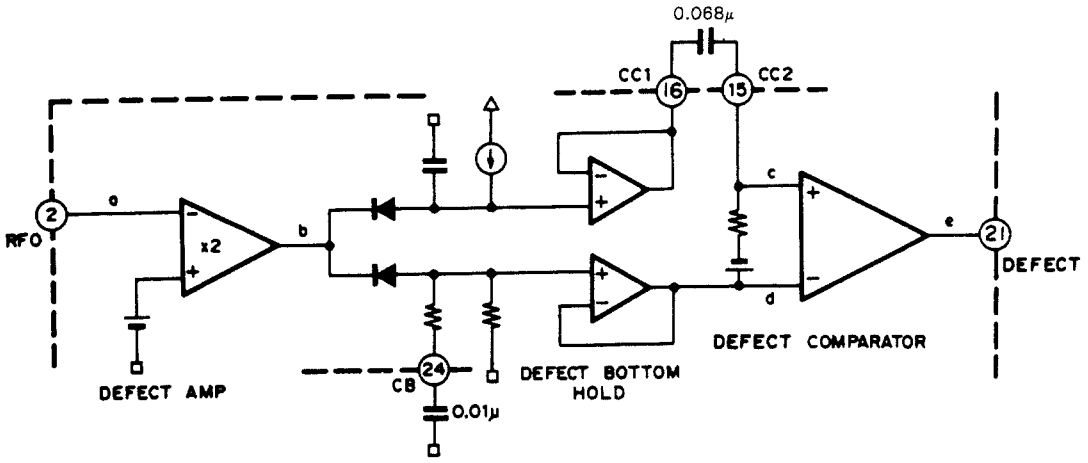
R186, R221, C147 and C160 constitute a LPF to obtain the DC component of (Vcc + DGND)/2 (V). If the cut-off frequency (fc) is set to more than 500Hz, leakage of the EFM low frequency signals will be greatly increased and will result in a degradation of the block error rate.



- **Defect circuit**

After inverting the RFI signal, the defect circuit bottom holds with the two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generates the mirror defect detecting signals.





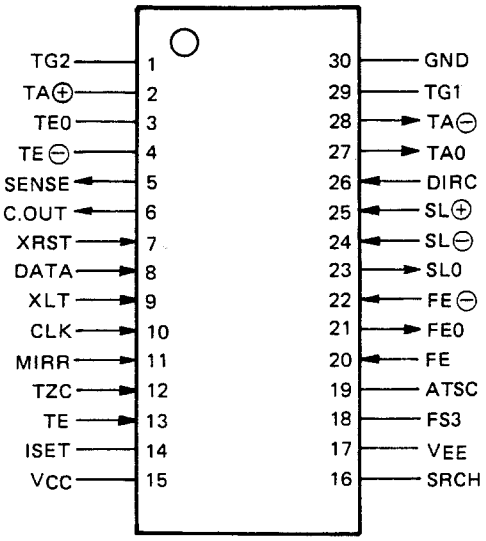
CIRCUIT DESCRIPTION

IC19: CXA1244S (X25-3120-11)
Servo signal processor

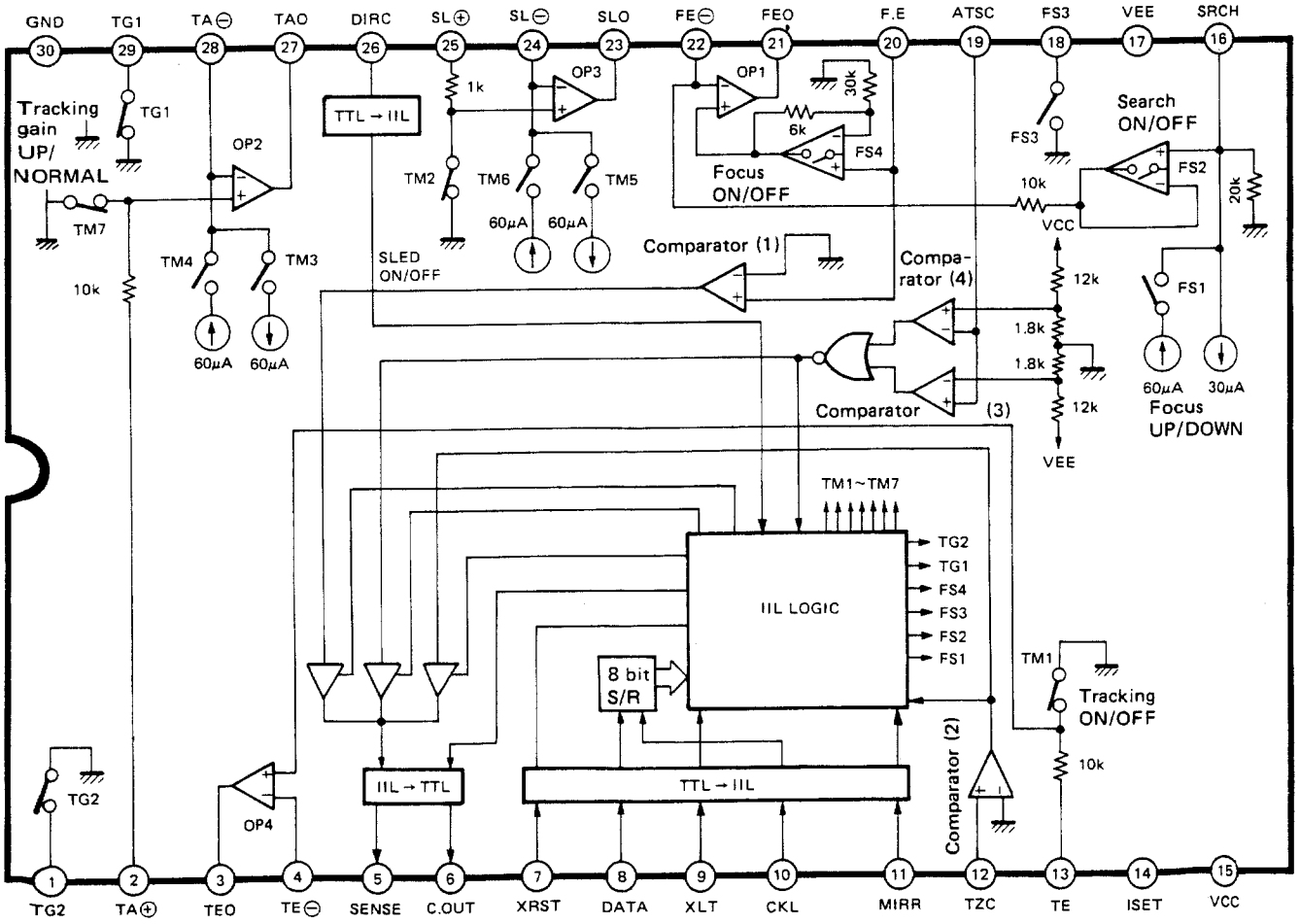
CX1244S is a bipolar IC developed for servo fo compact disc (CD) players, and it provides the following functions.

- ○Focus control (search ON/OFF, gain control)
- ○Tracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- ○ Sled control (servo ON/OFF, fast forward, fast reverse)

Terminal connection diagram



Block diagram



CIRCUIT DESCRIPTION

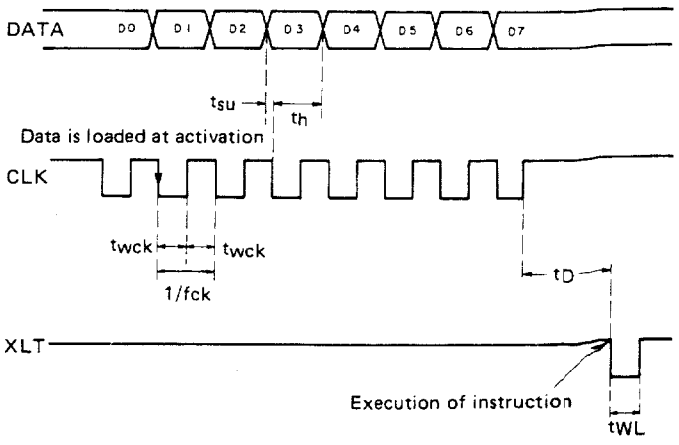
Explanation of terminals

Terminal No.	Terminal name	I/O	Functions
1	TG2		Tracking amplifier gain switching terminal. GND level.
2	TA ⊕		Non-inverted input of operational amplifier 2.
3	TE0		Output of operational amplifier 4.
4	TE ⊖	O	Inverted input of operational amplifier 4.
5	SENSE	O	Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1.
6	C. OUT	O	Signal output for counting number of tracks at the time of high speed access.
7	XRST	I	All internal registers are cleared when CPU → SSP "L". Connected with CPU RESET. See Note 2.
8	DATA	I	Serial data transmission of CPU → SSP. Input is made from LSB. D0~D7.
9	XLT	I	Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced.
10	CLK	I	CPU → SSP serial data transmission block. Data is read at falling. "H" level before and after transmission.
11	MIRR	I	Mirror signal input from RF amplifier.
12	TZC	I	Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz.
13	TE	I	Tracking error signal input.
14	ISET		Setting of current level for determining focus search voltage, tracking jump voltage and thread feed voltage.
15	Vcc		Power supply terminal. Normally −5V.
16	SRCH		The condenser for determining the time constant of charge/discharge waveform for focus search is connected.
17	VEE		Power supply terminal. Normally −5V.
18	FS3		Focus amplifier gain switching terminal. GND level.
19	ATSC		Such information that a mechanical shock was applied to the player is input. Simply, a trakcing error is input through BPF. In this equipment it is connected to GND level and is not used.
20	FE	I	Input of focus error signal.
21	FE0	O	Output of operational amplifier 1.
22	FE ⊖	I	Inverted input of operational amplifier 1.
23	SL0	O	Output of operational output 3.
24	SL ⊖	I	Inverted input of operational amplifier 3.
25	SL ⊕	I	Non-inverted input of operational amplifier 3.
26	DIRC	I	Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H". "L" for a fixed length of time with detection of activation, deactivation of TZC.
27	TA0	O	Output of operational amplifier 2.
28	TA ⊖	O	Inverted input of operational amplifier 2.
29	TG1		Tracking amplifier gain switching terminal. GND level.
30	GND		GND terminal of IC.

Note 1 : SENSE terminal output

Serial data upper 4 bits	ADDRESS content	SENSE terminal output	Explanation
0 0 0 0	FOCUS CONTROL	FZC	"H" when focus zero cross, Focus erro voltage is 0V or higher. Used at the time of FOCUS PULL operation.
0 0 0 1	TRACKING CONTROL	AS	"H" when the ATSC input level exceeds the wind comparator level (VTH = ±Vcc x 13%). But this is not used in this equipment.
0 0 1 0	TRACKING MODE	TZC	Judgement output of positive or negative of tracking zero cross, tracking error. When used at the time of single track jump, DIRC is reduced to "L" on detection of TZC ↑, in FWD JUMP or on detection of TZC ↓ in REV JUMP.

Note 2 : Digital unit timing chart



CIRCUIT DESCRIPTION

System control

COMMAND	ADDRESS				DATA				SENSE
	D7	D6	D5	D4	D3	D2	D1	D0	
FOCUS CONTROL	0	0	0	0	FS4 FOCUS ON	FS3 GAIN DOWN	FS2 SEARCH ON	FS1 SEARCH UP	FZC
TRACKING CONTROL	0	0	0	1	ANTI SHOCK	BREAK ON	TG2 GAIN	TG1* SET	AS
TRACKING MODE	0	0	1	0	TRACKING* MODE		SLED* MODE		TZC

GAIN SET* TG1, TG2 may be set independently.
In the case of ANTI SHOCK = 1 (00011XXX), both TG1, TG2 are inverted when ANTI SCHOCK = "H".

TRACKING MODE*

	D3	D2
OFF	0	0
SERVO ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

SLED MODE*

	D1	D0
OFF	0	0
SERVO ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

Note : The antishock circuit is not used in this equipment.

CIRCUIT DESCRIPTION

Serial data truth value table.

Serial data	Hexa-decimal	Function
FOCUS CONTROL		FS = 4321
00000000	S00	0000
00000001	S01	0001
00000010	S02	0010
00000011	S03	0011
00000100	S04	0100
00000101	S05	0101
00000110	S06	0110
00000111	S07	0111
00001000	S08	1000
00001001	S09	1001
00001010	S0A	1010
00001011	S0B	1011
00001100	S0C	1100
00001101	S0D	1101
00001110	S0E	1110
00001111	S0F	1111

TRACKING CONTROL		D2 (Brake)	AS = 0 TG = 2 1	AS = 1 TG = 2 1
00010000	S10	0	0 0	0 0
00010001	S11	0	0 1	0 1
00010010	S12	0	1 0	1 0
00010011	S13	0	1 1	1 1
00010100	S14	1	0 0	0 0
00010101	S15	1	0 1	0 1
00010110	S16	1	1 0	1 0
00010111	S17	1	1 1	1 1
00011000	S18	0	0 0	1 1
00011001	S19	0	0 1	1 0
00011010	S1A	0	1 0	0 1
00011011	S1B	0	1 1	0 0
00011100	S1C	1	0 0	1 1
00011101	S1D	1	0 1	1 0
00011110	S1E	1	1 0	0 1
00011111	S1F	1	1 1	0 0

AS : ANTI SHOCK

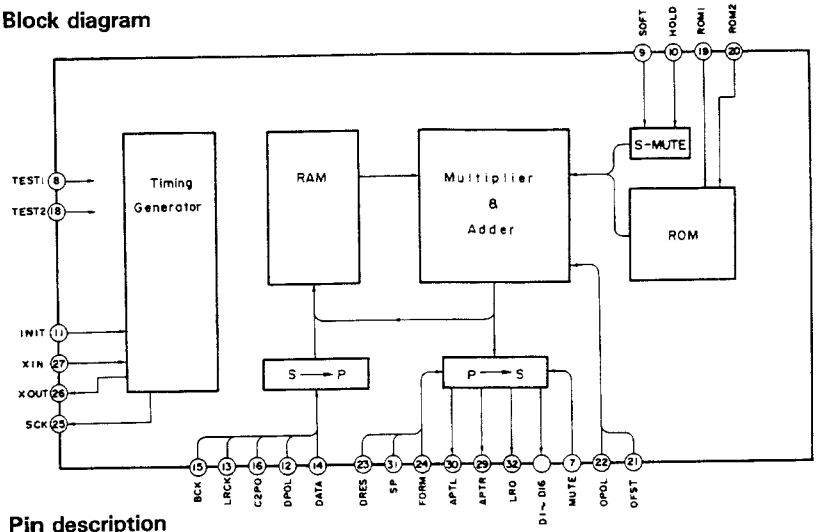
TRACKING MODE		DC = 1 TM = 654321	DC = 1 654321	DC = 1 654321
00100000	S20	000000	001000	000011
00100001	S21	000010	001010	000011
00100010	S22	010000	011000	100001
00100011	S23	100000	101000	100001
00100100	S24	000001	000100	000011
00100101	S25	000011	000110	000011
00100110	S26	010001	010100	100001
00100111	S27	100001	100100	100001
00101000	S28	000100	001000	000001
00101001	S29	000110	001010	000011
00101010	S2A	010100	011000	100001
00101011	S2B	100100	101000	100001
00101100	S2C	001000	000100	000011
00101101	S2D	001010	000110	000011
00101110	S2E	011000	010100	100001
00101111	S2F	101000	100100	100001

DC : DIRC input terminal

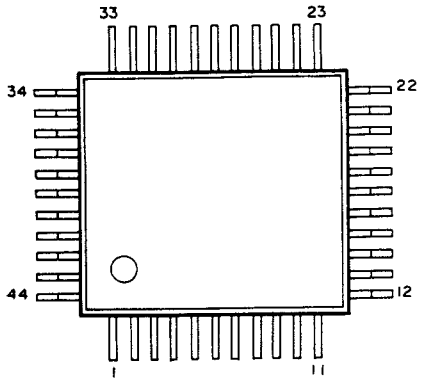
CIRCUIT DESCRIPTION

IC13: CXD1088Q (X25-3120-11) Digital filter

Block diagram



Pin arrangement (Top view)

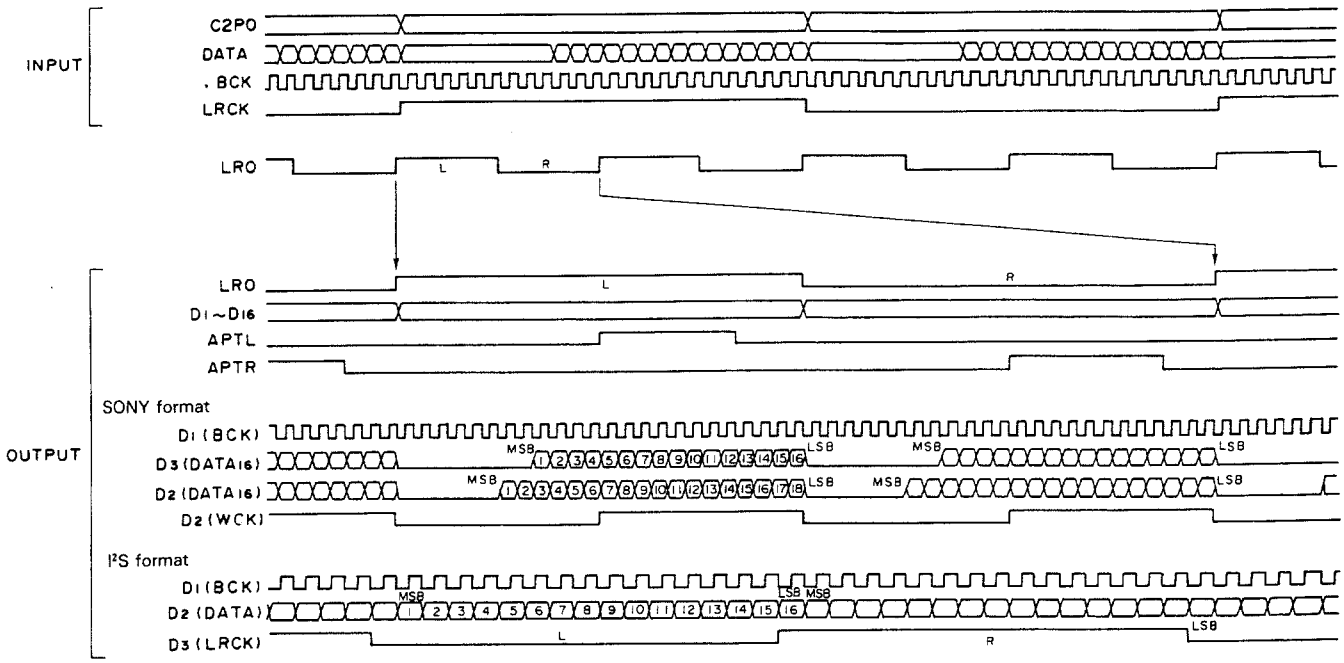


Pin description

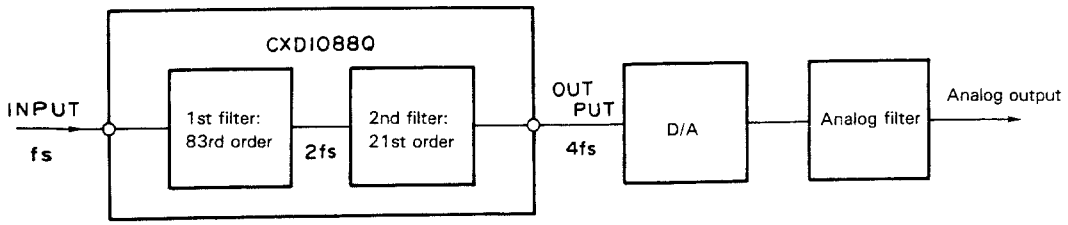
Pin No.	Pin Symbol	I/O	Pin Function
1 ~ 5	D_{12} ~ D_{16}	O	D_{12} ~ D_{16} output in parallel mode. Fixed at low level in serial mode.
6	V_{SS}	—	Negative power supply (0 V)
7	MUTE	I	Sets output to "0" or offset value. Active high.
8	TEST1	I	Test pin. Fixed at low level in normal use.
9	SOFT	I	Soft muting ON/OFF. Mute ON at high.
10	HOLD	I	Stops muting operation. Stops at high.
11	INIT	I	Power ON reset input. Active low.
12	DPOL	I	Inverts polarity of input data
13	LRCK	I	LRCK input
14	DATA	I	16-bit × 2 serial mode data input. 2's complement
15	BCK	I	BCK input
16	C2PO	I	Error flag input
17	V_{DD}	—	Positive power supply (+5 V)
18	TEST2	I	Test pin. Fixed at low level in normal use.
19	ROM1	I	ROM select for 83rd order
20	ROM2	I	ROM select for 21st order
21	OFST	I	Adds offset to output. Active high.
22	OPOL	I	Specifies polarity of offset value. High (+1%), Low (−1%)
23	DRES	I	Data word length in SONY format serial mode output High: 18 bits, Low: 16 bits
24	FORM	I	Specifies output format. High: I²S Low: SONY
25	SCK	O	System clock output for external IC (384 fs)
26	XOUT	O	Crystal oscillator output (384 fs)
27	XIN	I	Crystal oscillator input (384 fs)
28	V_{SS}	—	Negative power supply (0 V)
29	APTR	O	Aperture clock for R-channel
30	APTL	O	Aperture clock for L-channel
31	SP	I	Serial/parallel mode output select. High: parallel mode, Low: serial mode
32	LRO	O	LRCK output (4 fs)
33	D_1	O	D_1 (MSB) output in parallel mode. BCK output in serial mode. (4 fs)
34	D_2	O	D_2 output in parallel mode. DATA output in serial mode. (4 fs)
35	D_3	O	D_3 output in parallel mode. Serial: LRCK output (I²S mode), WCK output (SONY mode)
36 ~ 38	D_4 ~ D_6	O	D_4 ~ D_6 output in parallel mode. Fixed at low level in serial mode.
39	V_{DD}	—	Positive power supply (+5 V)
40 ~ 44	D_7 ~ D_{11}	O	D_7 ~ D_{11} output in parallel mode. Fixed at low level in serial mode.

CIRCUIT DESCRIPTION

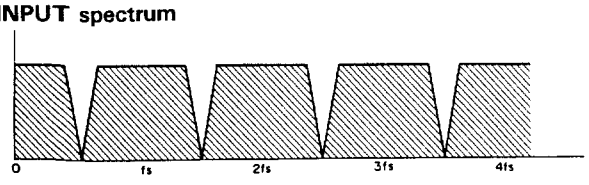
Input/output timing chart



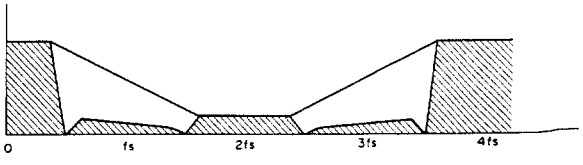
Filter characteristics



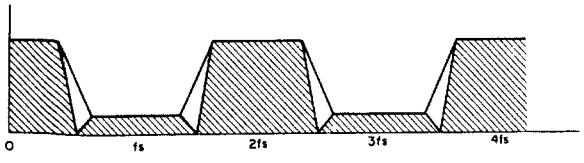
INPUT spectrum



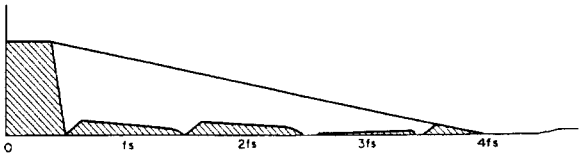
2nd filter characteristics



1st filter characteristics



Analog filter characteristics



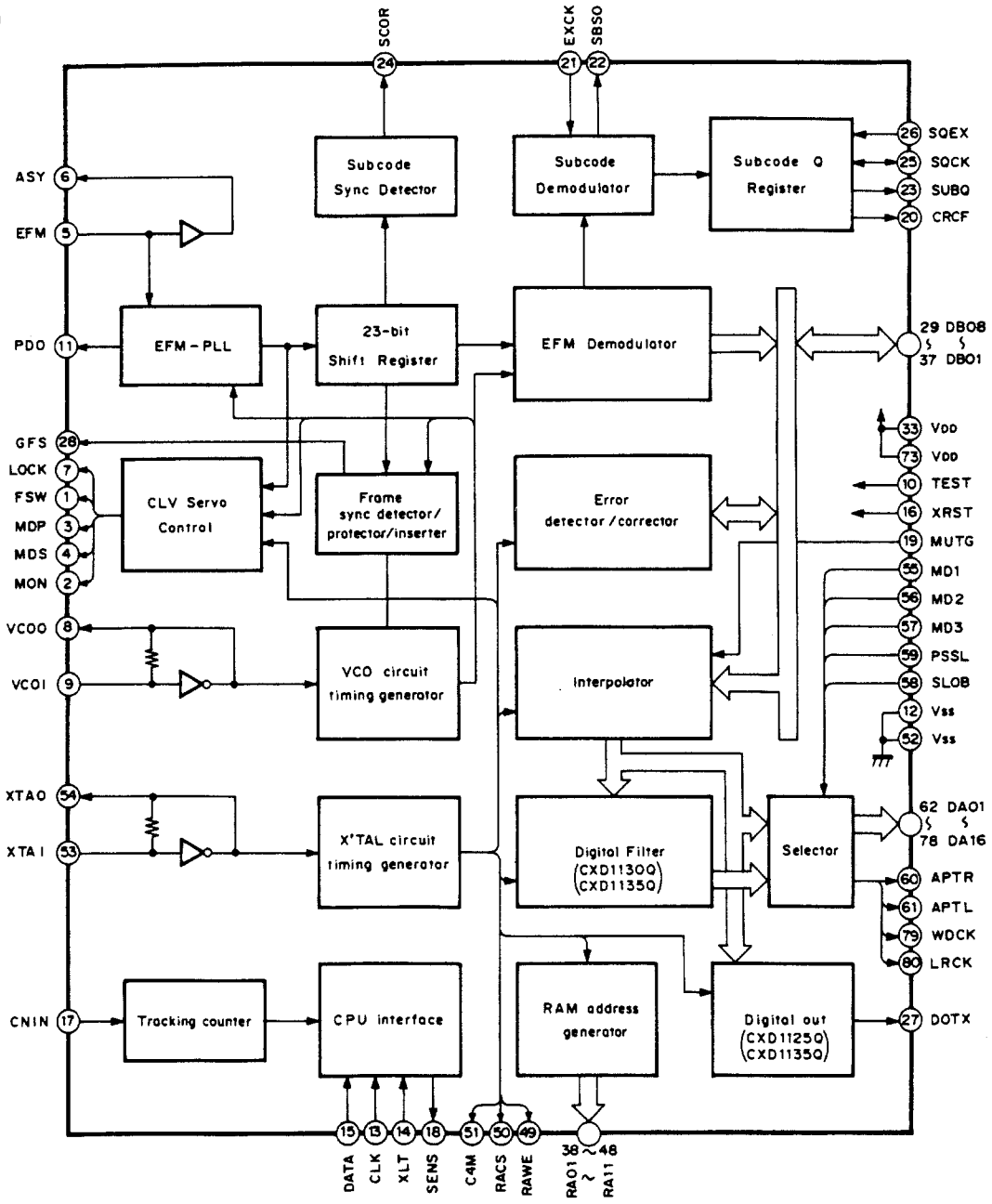
CIRCUIT DESCRIPTION

IC14: CXD1125Q (X25-3120-11) Digital signal processing LSI

The CXD1125Q is the digital signal processing LSI for the compact disc player, and has the following functions. All the digital signals for reproduction can be processed internally with this one-chip design.

- Bit clock reproduction by an EFM-PLL circuit.
- EFM data demodulation.
- Frame sync signal detection, protection and insertion.
- Powerful error detection and correction.
- Interpolation with average value or by holding the previous value.
- Demodulaiton of sub code signal or error detection of sub code Q.
- Spindle motor CLV servo.
- 8-bit tracking counter.
- CPU interface with a serial bus.
- Sub code Q register.
- D/A interface output.

Block diagram



CIRCUIT DESCRIPTION

Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in arow, outputs "L".
8	VCOO	O	VCO output. f = 8.6436MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	Vss	–	GND (0V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENSE	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case where ATTM of internal register A is "L". normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code Q read-off clock.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync SO + SI output.
25	WFCK	O	Write Frame Clock output. f = 7.35kHz when the frame sync is locked.
28	CFS	O	Output of display of lock status of frame sync.
29	DB08	I/O	Data terminal of external RAM. DATA 8 (MSB)
30	DB07	I/O	Data terminal of external RAM. DATA 7
31	DB06	I/O	Data terminal of external RAM. DATA 6
32	DB05	I/O	Data terminal of external RAM. DATA 5
33	VDD	–	Power supply (+ 5V)
34	DB04	I/O	Data terminal of external RAM. DATA 4
35	DB03	I/O	Data terminal of external RAM. DATA 3
36	DB02	I/O	Data terminal of external RAM. DATA 2
37	DB01	I/O	Data terminal of external RAM. DATA 1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (active at "L").
50	RACS	O	Chip select signal output to external RAM. (active at "L").

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
51	C4M	O	Crystal dividing output. f = 4.2336MHz.
52	Vss	–	GND (0V).
53	XTAI	I	Crystal oscillator input. f = 8.4672MHz or 16.9344MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f = 8.4672MHz or 16.9344MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select output. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL = "H", C1F1 output when PSSL = "L".
63	DA02	O	DA02 output when PSSL = "H", C1F2 output when PSSL = "L".
64	DA03	O	DA03 output when PSSL = "H", C2F1 output when PSSL = "L".
65	DA04	O	DA04 output when PSSL = "H", C2F2 output when PSSL = "L".
66	DA05	O	DA05 output when PSSL = "H", C2FL output when PSSL = "L".
67	DA06	O	DA06 output when PSSL = "H", C2PO output when PSSL = "L".
68	DA07	O	DA07 output when PSSL = "H", RFCK output when PSSL = "L".
69	DA08	O	DA08 output when PSSL = "H", WFCK output when PSSL = "L".
70	DA09	O	DA09 output when PSSL = "H", $\overline{\text{PLCK}}$ output when PSSL = "L".
71	DA10	O	DA10 output when PSSL = "H", UGFS output when PSSL = "L".
72	DA11	O	DA11 output when PSSL = "H", GTOP output when PSSL = "L".
73	VDD	–	Power supply (+ 5V).
74	DA12	O	DA12 output when PSSL = "H", RAOV output when PSSL = "L".
75	DA13	O	DA13 output when PSSL = "H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL = "H", $\overline{\text{C21O}}$ output when PSSL = "L".
77	DA15	O	DA15 output when PSSL = "H", C21O output when PSSL = "L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL = "H", DATA output when PSSL = "L".
79	WDCK	O	Strobe signal output. 88.2kHz.
80	LRCK	O	Strobe signal output. 44.1kHz.

Notes:

C1F1 : } Error correction status monitor output for C1 decode.
C1F2 : }

C2F1 : } Error correction status monitor output for C2 decode.
C2F2 : }

C2PO : C2 pointer signal.

C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

RFCK : Read frame clock output. 7.35MHz when locked to the crystal line.

WFCK : Write frame clock output. 7.35MHz when locked to the crystal line.

$\overline{\text{PLCK}}$: VCO/2 output. f = 4.3218MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.

C4LR : Strobe signal. 176.4kHz.

$\overline{\text{C21O}}$: C21O invert output.

C21O : Bit clock output. 2.1168MHz.

DATA : Audio signal serial data output.

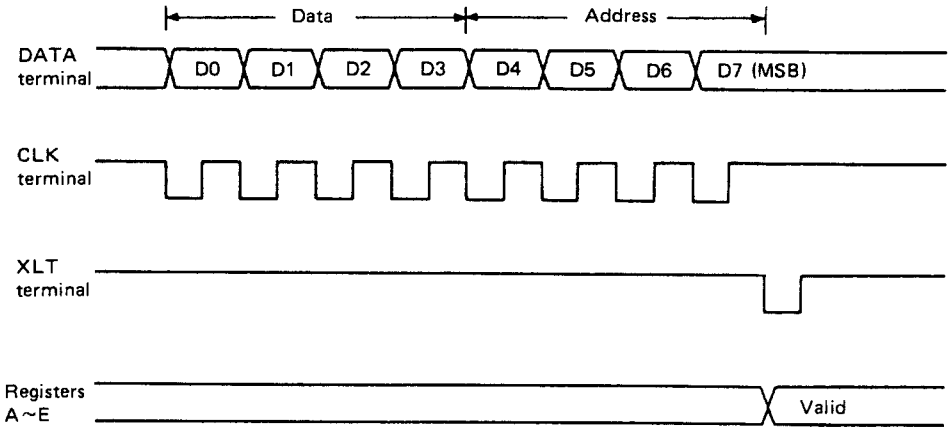
CIRCUIT DESCRIPTION

Explanation of functions

- **CPU interface**

1) Data input

Each register may be set by input of 4 bit address, and 4 bit data from LSB in the timing that is shown in Fig. to three terminals, XLT, CLK and DATA. The address and data of each terminal are as shown in Table and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".



Timing chart for data input

2) Registers

○ Register 9 – New function control

Controls the new functions added to the CX23035.

D3 : ZCMT Switches the zero cross mute function ON/OFF. Details are described in **"Interpolation and Mute, Attenuate"**.

D2 : HZPD One of the defect countermeasures. Switches ON/OFF the function which makes the PDO pin a high impedance (Z) for a maximum of 0.55ms from the rising edge of GFS. Details are described in **"Countermeasures to defects"**.

D1 : NCLV Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in **"CLV servo control"**.

D0 : CRCQ Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in **"5) Subcode output"**.

○ Register A – Sync. protection, attenuator control

D3 : GSEM
D2 : GSEL
D1 : WSEL
D0 : ATTM

Provided for switching frame synk. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of **"EFM demodulation"**.

D0 : ATTM Used for attenuating audio signals by 12dB, and the details will be described in the paragraph of **"D/A interface"**.

○ Registers B and C – Counter set, more significant 4 bits (register C) and less significant 4 bits (register B)

these registers are used for setting the tracking count value. the data of registers B and C are preset in the counter through the 4 bit buffer register assigned by address. Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8 bit data (either buffer register is of "OLD" data.)

D3 : DIV The dividing ratio of RFCK and WFCK in CLV-P mode is fixed, and the phase is compared with RFCK/4 or WFCK/4 respectively, regardless of the status of D3, then output from the MDP pin.

○ Register D-CLV control

D3 : DIV Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0,, phase comparison of RFCK/4 and WFCK/4 is made, and when D3 = 1, phase comparison of RFCK/8 and WFCK/8 is made, and output is made out of MDP terminal in each case.

D2 : TB Used for determining the period of bottom hold in the CLV-S and CLV-H modes. Bottom hold is made in the period of RFCK /32 when D2 = 0 or in the period of RFCK/16 when D2 = 1.

D1 : Tp Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D0 : GAIN Used for setting the gain of MDP terminal output in the CLV-S and CLV-H modes. It is –12dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0dB when D0 = 1.

CIRCUIT DESCRIPTION

○ Register E-CLV mode

It is as shown in Table.

The details of each mode will be described in the paragraph of CLV servo control.

Register name	Command	Address D7~D4	Data D3	D2	D1	D0	SENSE terminal
9*1	New function control	1 0 0 1	ZCMT	HZPD	NCLV	CRCQ	Z
A*2	Sync protection, attenuator control	1 0 1 0	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4 bits	1 0 1 1	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, More significant 4 bits	1 1 0 0	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D*3	CLV control	1 1 0 1	DIV	TB	TP	GAIN	Z
E*4	CLV mode	1 1 1 0		CLV mode			$\overline{\text{Pw} \geqq 64}$

***1 Register 9**

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDC pin is always active	PDC pin is "Z" at the trailing edge of GFS
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

***2 Register A**

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG terminal	dB
0	0	0
0	1	$-\infty$
1	0	−12
1	1	−12

***3 Register D**

DIV	D3	0	RFCK/4 & WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8 & WFCK/8	
TB	D2	0	RFCK/32	Bottom hold period in CLV-S, CLV-H mode
		1	RFCK/16	
TP	D1	0	RFCK/4	Peak hold frequency in CLV-S mode
		1	RFCK/2	
GAIN	D0	0	−12dB	Gain at MDP terminal in CLV-S, CLV-H mode
		1	0dB	

***4 Register E**

Mode	D3~D0	MDP terminal	MDS terminal	FSW terminal	MON terminal
STOP	0 0 0 0	L	Z	L	L
KICK	1 0 0 0	H	Z	L	H
BRAKE	1 0 1 0	L	Z	L	H
CLV-S	1 1 1 0	CLV-S	Z	L	H
CLV-H	1 1 0 0	CLV-H	Z	L	H
CLV-P	1 1 1 1	CLV-P	CLV-P	Z	H
CLV-A	0 1 1 0	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Ż : High impedance

List of registers

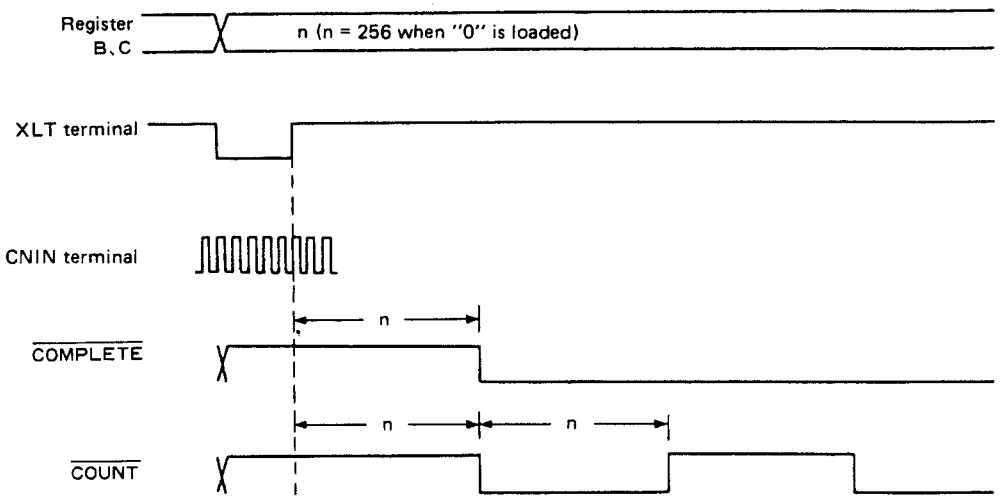
CIRCUIT DESCRIPTION

3) Trakcing counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in register B and C. Count of CNIN pulses is started at raising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal ($\overline{\text{COMPLETE}}$) that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENSE terminal. When the address is set at "C", signal ($\overline{\text{COUNT}}$) of CNIN/2n (Hz) is output.

The tracking counter timing chart is shown in Fig.



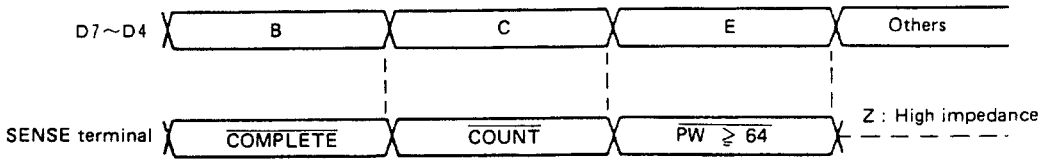
Tracking counter timing chart

4) SENSE

The following signals are output from SENSE terminal depending on the address of D7~D4.

1. $\overline{\text{COMPLETE}}$: Address is "B"; Shown in Fig.
2. $\overline{\text{COUNT}}$: Address is "C"; Shown in Fig.
3. $\overline{\text{PW}\geqq 64}$: Address is "E"; this signal is of LOW level when the pulse width after bottom hold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note : Address setting is determined only by the data that corresponds to D4~D7 which can be input from DATA terminal shown in Fig.



Timing chart of SENSE terminal

CIRCUIT DESCRIPTION

5) Sub code output

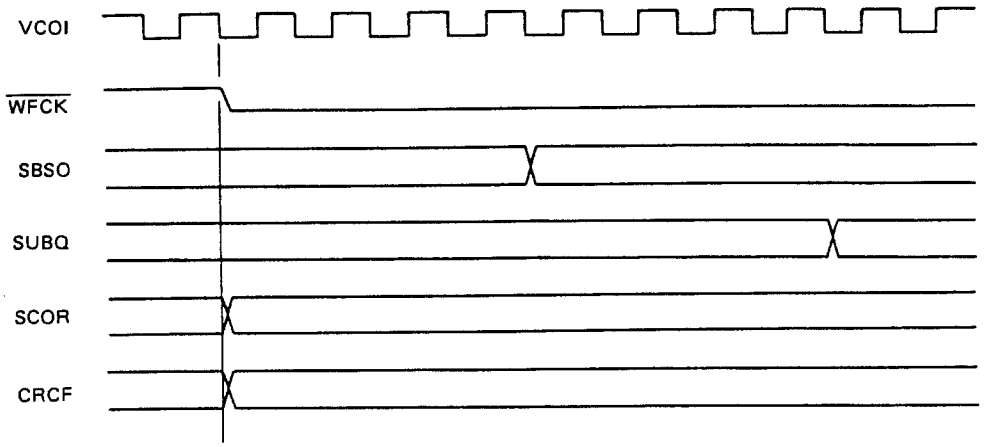
Sub codes P~W loaded in the 8 bit shift register are output out of SBSO terminal in accordance with the clock input through EXCK terminal. when SCOR terminal is "H", S0 · S1 signal is output.

Sub code Q is as follows, depending on the SQEX pin status.

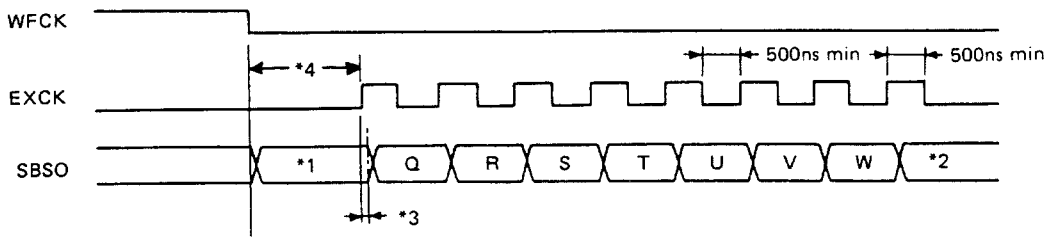
(i) When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The WFCK is also output from the SQCK pin.

(ii) When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock (as from the microprocessor). Two 80-bit shift registers, for reading and writing, are incorporated, and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF = "H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4 bits, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4 bits of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF



(b) Timing of SBSO, EXCK



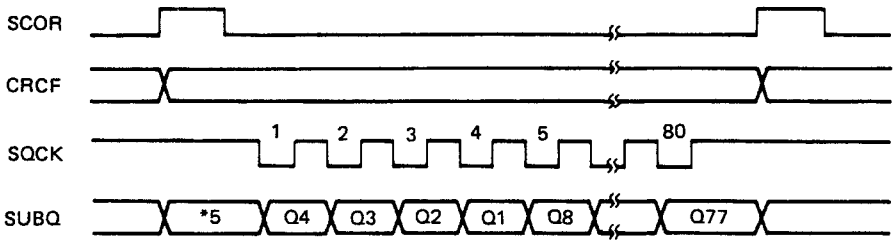
*1 : Sub code P is output when SCOR is 0.
S0 · S1 is output when SCOR is 1.
*2 : SBSO is 0 when 8 or more pulses are input to EXCK.
*3 : 4T ~ 6T if the period of VCO is expressed as T.
*4 : Make EXCK low for 10μs from the rising edge of WFCK.
One time period of T = 8.6436MHz.

(1) Timing chart of sub code outputs

CIRCUIT DESCRIPTION

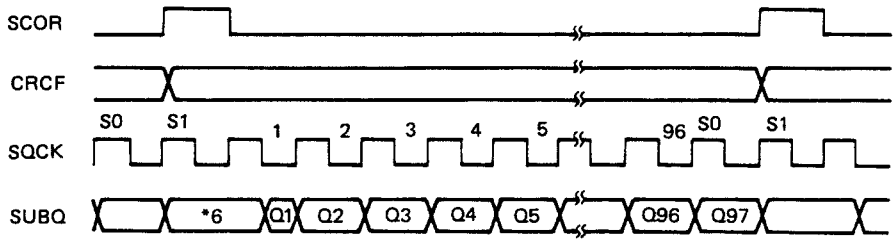
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX= "H" level



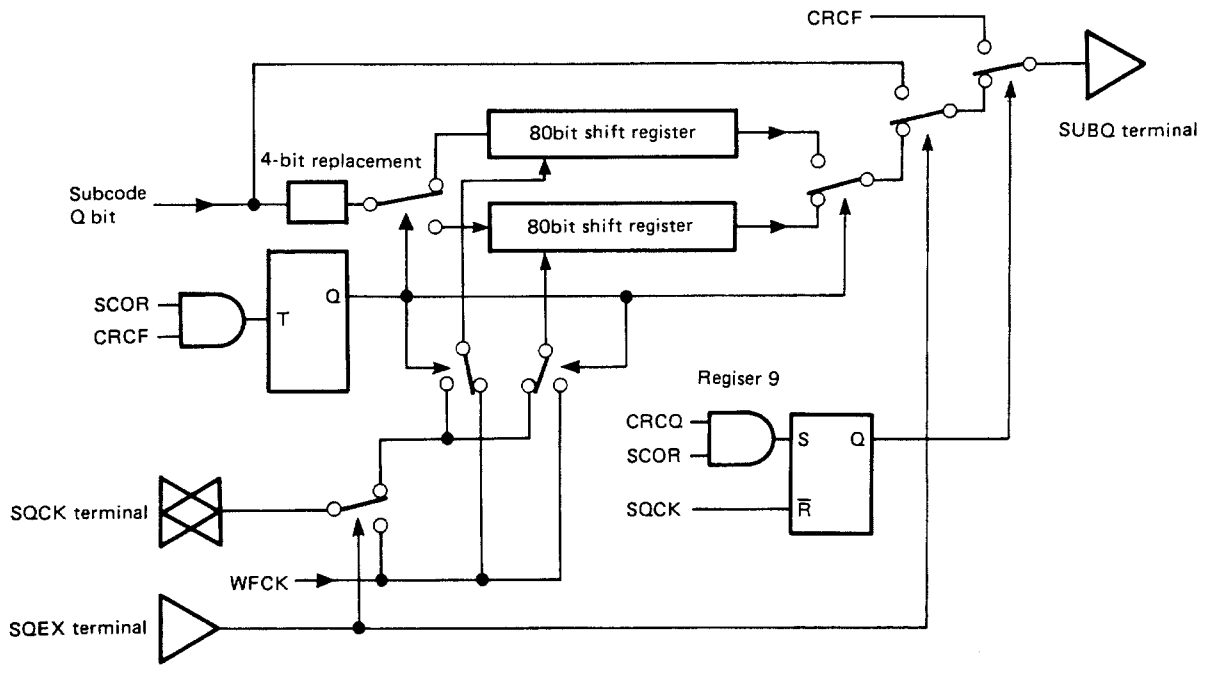
*5 : CRCF when CRCQ flag is "1", undefined when "0".

SQEX= "L" level



*6 : CRCF when CRCQ flag is "1", Q98,Q1 when "0".

(2) Timing chart of sub code outputs



CIRCUIT DESCRIPTION

- **EFM demodulation**

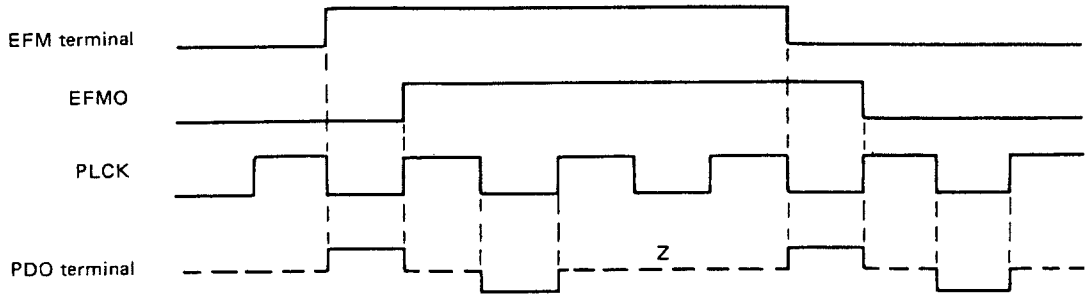
1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32MHz synchronized with this clock by the EFM-PLL circuit.

At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO terminal. The mean value of PDO terminal is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

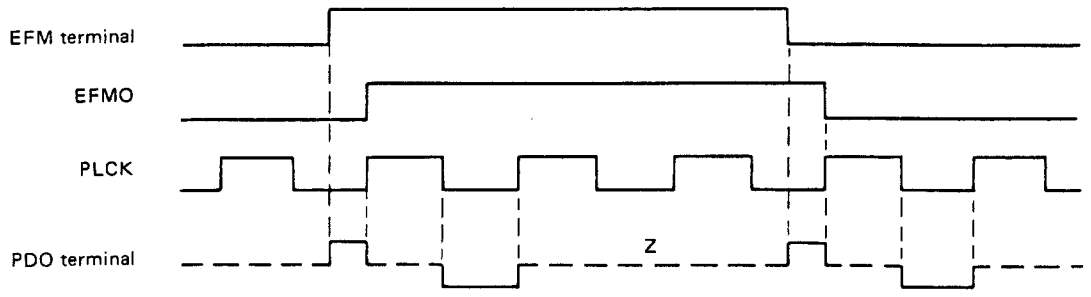
The timing charts of EFM terminal, EFMO, PLCK and PDO are shown in Fig.

(a) When EFM signal and VCO are synchronized



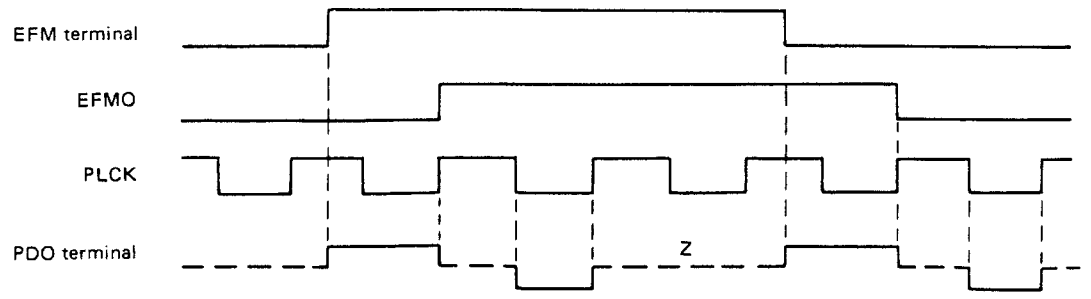
Z : High impedance

(b) When VCO is higher than EFM signal



Z : High impedance

(c) When VCO is less than EFM signal



Z : High impedance

Timing charts of EFM-PLL circuit

CIRCUIT DESCRIPTION

2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23 bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL. If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218MHz/588 = 7.35kHz)

A 4 bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4 bit counter is reset with the next frame synchronizing signal. the GTOP terminal is of "H" while this operation is performed. Further, GFS terminal is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the wondow is output out of UGFS (DA05 terminal at the time when PSSL = L.)

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frames to be interpolated	UGFS (PSSL = "L")
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ), Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

3) EFM demodulation

14 bit data is taken out of the 23 bit shift register and is demodulated to 8 bit data through 14 → 8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08~DB01) terminals) of the RAM in accordance with the OENB signal transmitted from said block.

- **Sub code demodulation**

1) Sub code demodulation

synchronizing signals S0, S1 of 14 bit sub codes are detected out of the 23 bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0 + S1 is output out of SCOR terminal and S0 · S1 is output out of SBSO terminal (only when SCOR = H.)

Data (P~W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output out of SUBQ terminal, and at the same time, it is loaded in the 8 bit shift register and is output out of SBSO terminal in correspondence to a clock from EXCK terminal.

The detials of this timing will be shown in the paragraph of CPU interface.

2) Sub code Q error detection

The CRC sub code result is output from the CRCF pin in synchronism with the SCOR pin. It goes "L" when an error is detected. At the same time as the CRCQ flag is "1", the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detialed in **"CPU interface"**.

CIRCUIT DESCRIPTION

- **RAM interface (generation of external RAM address)**

1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block, the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal. This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'Tal system are used for processing thereafter.

2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block. This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock C212 (8.4672MHz/4). The data output out of the RAM is C2 pointer first, less significant 8 bits out of 16 bits and finally more significant 8 bits.

3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data. In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8 bit data directed to the RAM interface block from the error correction block. The requests from the error correction unit are of the lowest priority among requests of three types. After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal. This block generates the address of the requested data, and controls R/W of the RAM at the same time.

4) Address generation

The data after EFM demodulation is data subjected to interleave processing. This interleave processing is subjected to data lag by the unit of a frame. Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer. The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Pointe R/W 65 times in one frame section
   The number of times of address generation to it is 129 times.

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum. In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are not accepted in this timing. When requests 2, 3 are generated simultaneously, priority is given to request 2, and if a requestis generated during execution of either request, priority is given to the job in execution.

CIRCUIT DESCRIPTION

6) Jitter margin

The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synmchronized with the clock of X'Tal system, this RAM is subjected to time axis correction.

However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.

In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter. As a result, there is no case where data without error correction is output to the D/A.

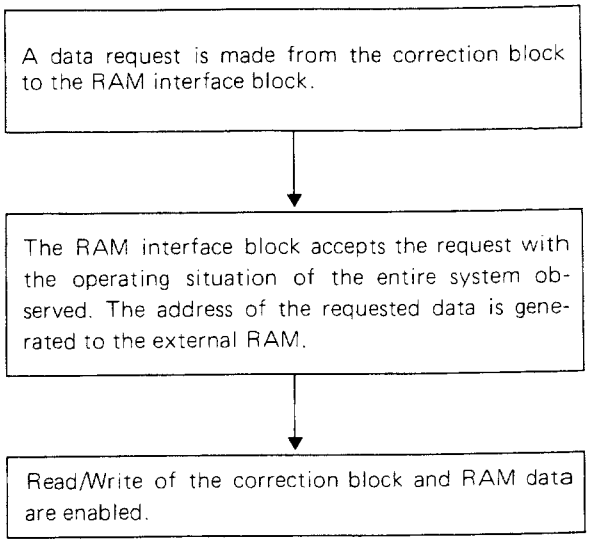
The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.

- **Error correction**

1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16k RAM stores these pointer data in addition to audio data.
3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16 bits).
6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.
7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" when a period of minimum 472ns after deactivation of terminal RFCK. C2FL is the AND of C2F1 and C2F2.

Note : 472ns : One period of 2.1168MHz

8) The flow of data with the external RAM is as follows.



9) When PSSL is set at "L", a signal that is capable of monitoring error correction is output. C1F1, C1F2, C2F2 output to DA01~DA04 are these monitor signals. This signal is reset to "L" when a period of minimum 472 ns has elapsed since deactivation of RFCK.

The levels and meanings of these signals at the time of deactivaiton of RFCK are as follows.

C1F1	C1F2	C1 correction status
0	0	No Error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No Error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

CIRCUIT DESCRIPTION

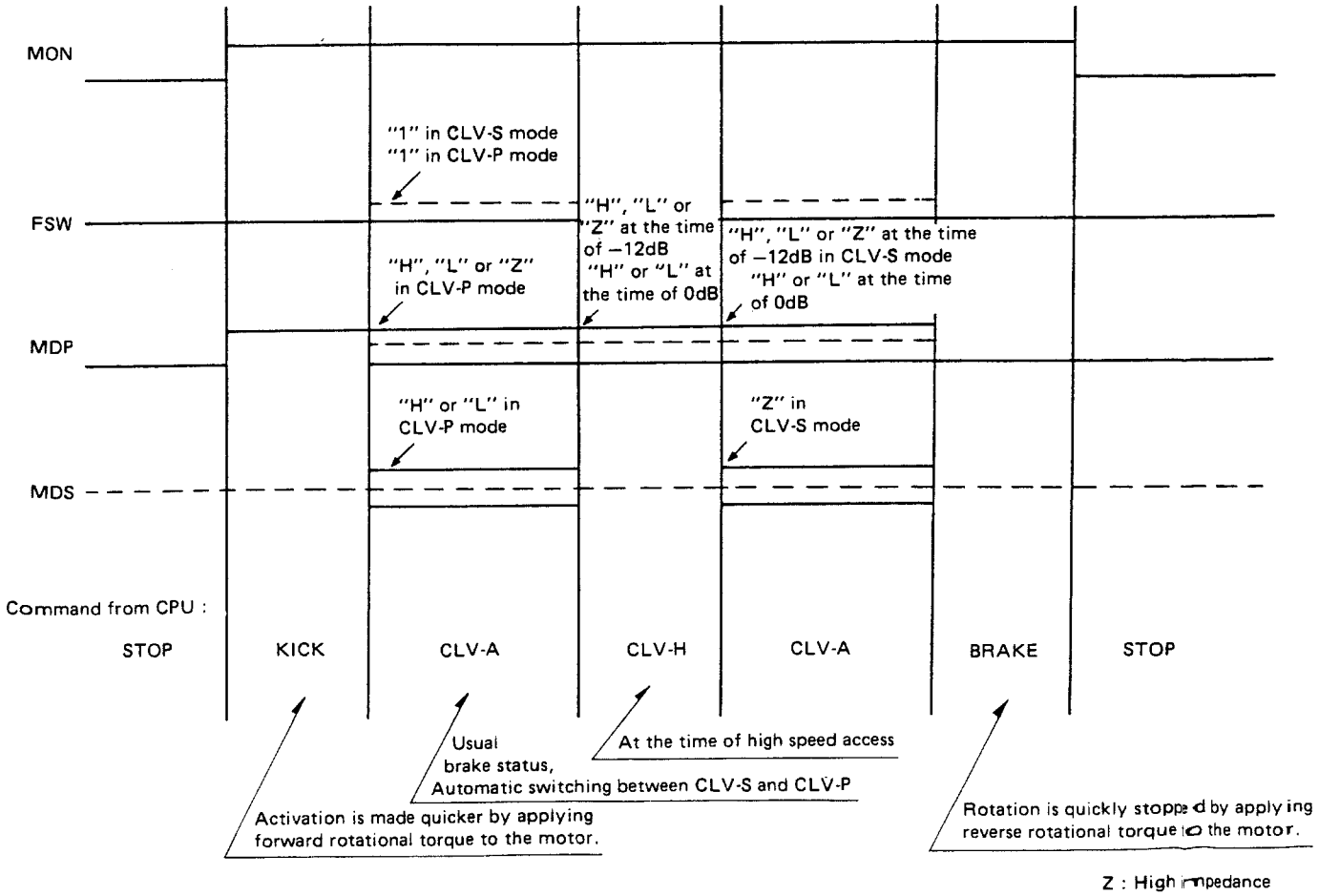
- **CLV servo control**

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP terminal for controlling synchronization of velocity and phase, MDS terminal for controlling synchronization of velocity, FSW terminal for making selection of filter constant and MON terminal for controlling motor ON/OFF.

1) STOP : Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"

2) KICK : Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".

3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".

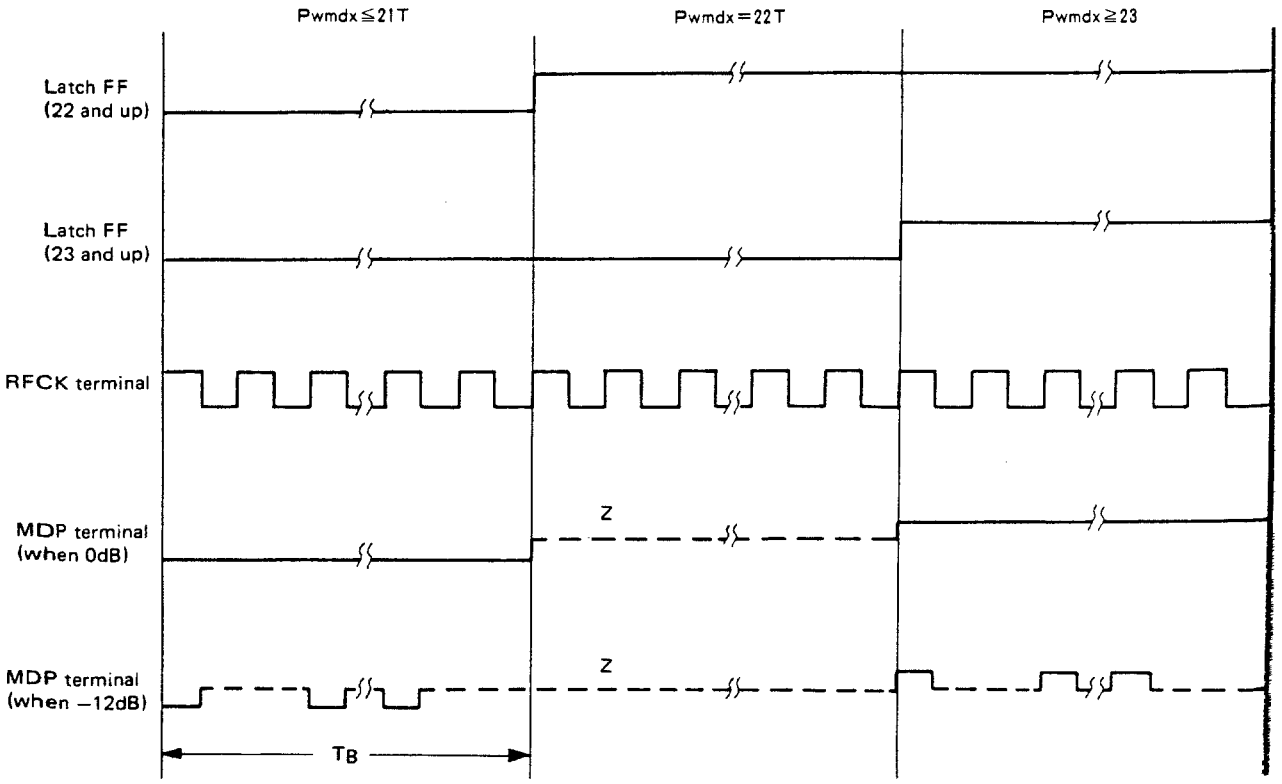


Typical control of spindle motor

CIRCUIT DESCRIPTION

4) CLV-S : Register E = 1100'B
Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason. When the period of VCO's oscillation frequency 8.6436MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practive, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulses are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal. "L" is produced out of MDS terminal while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more.
Either 0dB or 12dB can be selected as its gain.
MDS = "Z", FSW = "L", MON = "H".

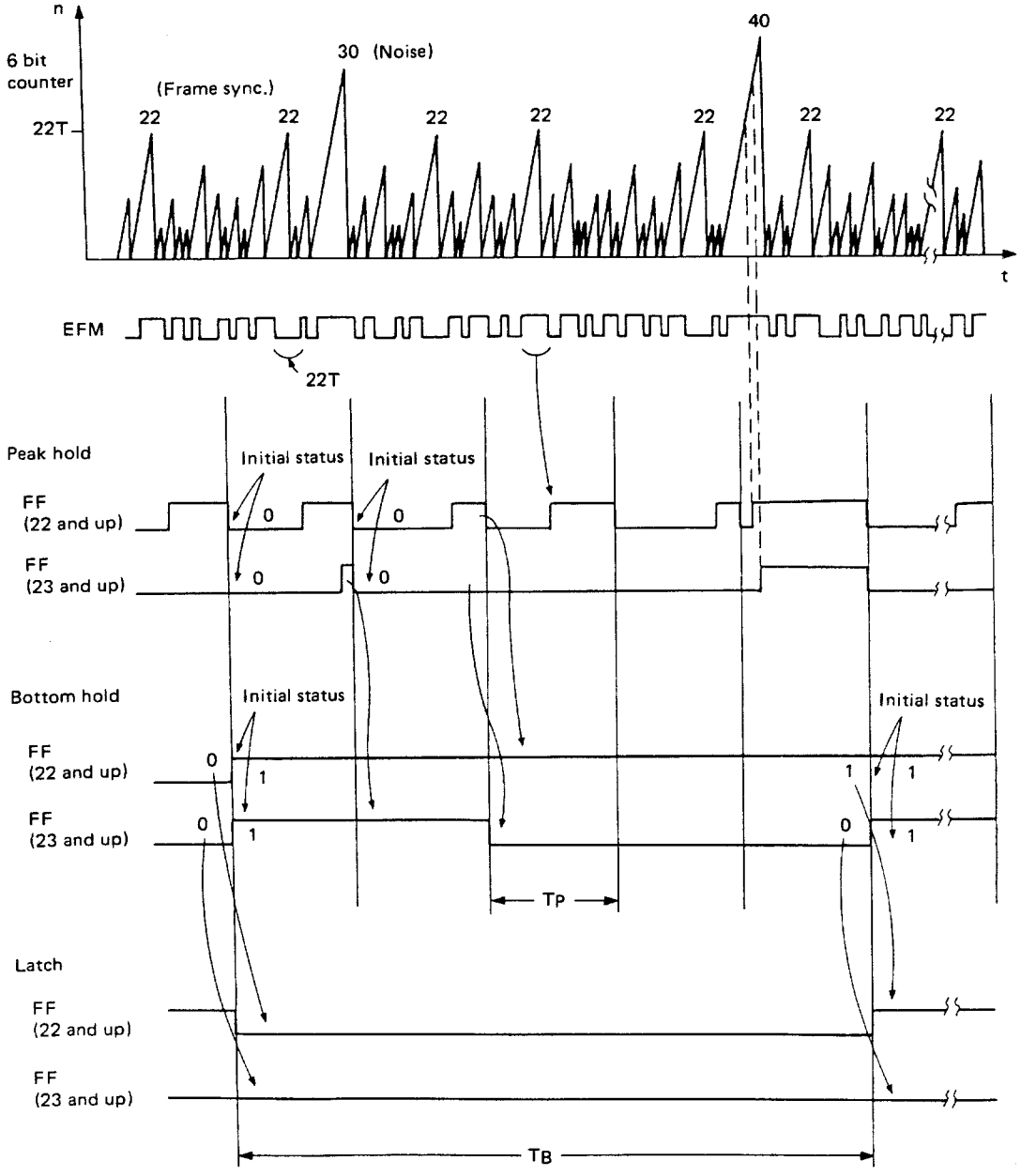
5) CLV-P: Register E = 1111'B
PLL servo mode.
When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized. If the 8.4672/2MHz period is T, and the time when WFCK is "H" is tHW, then the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by (tHW−279T) X 32, and then goes "L" until the next trailing edge of WFCK.
MDS $\leqq$ "H" when tHW = 279T,
MDS = "L" when tHW $\geqq$ 279T.
The MDS pin varies between 32T and 544T, in 32T steps, when 280T $\leqq$ tHW $\leqq$ 296T. For example, when synchronized (rotating at the standard speed), that is when tHW = 288T, a 7.35kHz signal, with a duty cycle of 50% is output.
FSW = "Z", MON = "H".



Timing chart in CLV-S, CLV-H mode (1)

CIRCUIT DESCRIPTION

TP : RFCK/2 or RFCK/4 in the case of CLV-S, F8M/256 in the case of CLV-H
TB : RFCK/16 or RFCK/32 in the case of CLV-S, CLV-H

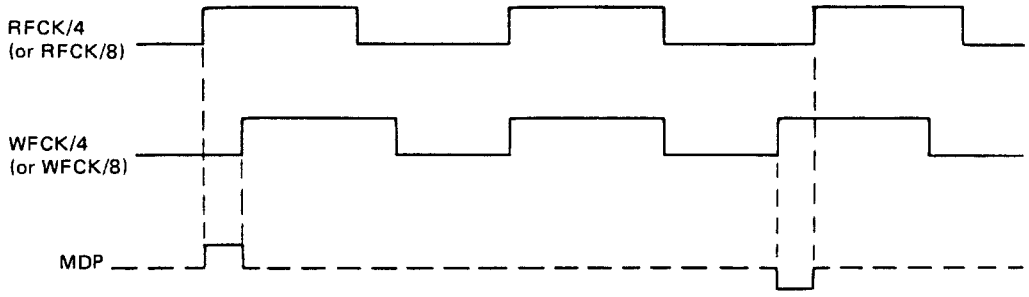


Timing chart in CLV-S, CLV-H mode (2)

CIRCUIT DESCRIPTION

6) CLV-P : Register E = 1111'B
PLL servo mode.
Phase comparison of signals WFCK/4 and RFCK/4 or WFCK/8 and RFCK/8 is made, and output is made out of MDP terminal. "H" when WFCK has delayed, "L" when WFCK is fast, and "Z" when synchronized. When the period of 8.4672/2MHz is expressed at T and the length of time when WFCK is "H" is expressed at tHW, such a signal that is of "H" during (tHW−279T) x 32 with 7.35kHz as a period and that is "L" during the remaining time is produced out of MDS terminal. MDS = "L" when tHW ≦ 279T. MDS = "H" when tHW ≦ 297T. When 280T ≦ tHW ≦ 296T, the MDS terminal changes in 32T steps from 32T to 544T. When synchronized, for instance, that is, when tHW = 288T, a signal of 7.35kHz of DUTY 50% is produced. FSW = "Z", MON = "H".

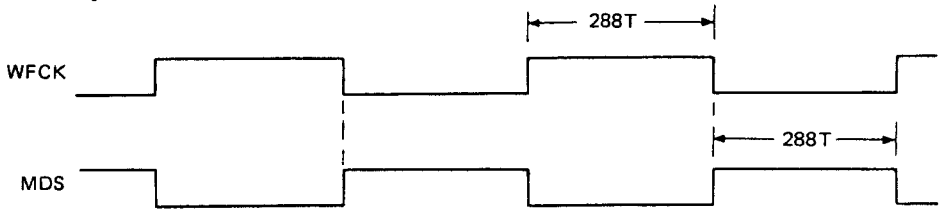
MDP terminal



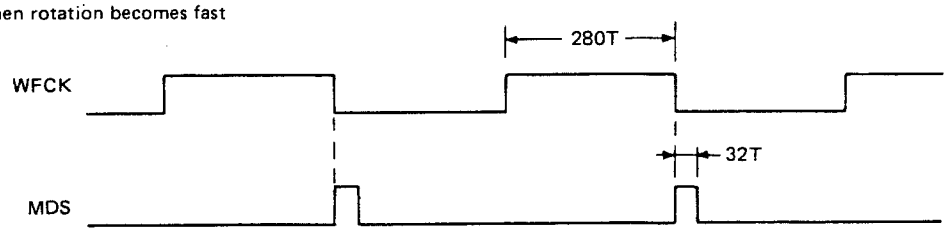
Z : High impedance

MDS terminal (The Period of 4.2336MHz is expressed as "T".)

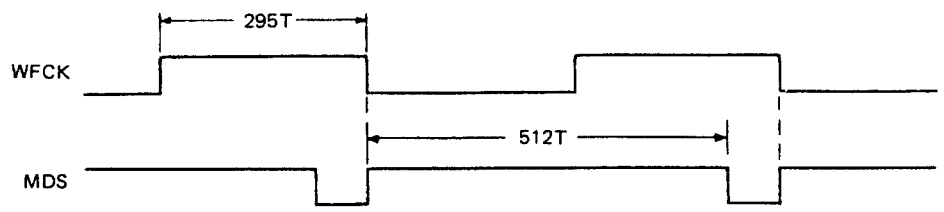
(1) When rotating at specified velocity



(2) When rotation becomes fast



(3) When rotation becomes slow



Timing chart in CLV-P mode

CIRCUIT DESCRIPTION

7) CLV-A: Register E = 0110'B

The mode used for normal play status.

The GFS signal ("H" when locked, "L" when unlocked), after frame sync detection, protection and insertion block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is "H". When the "L" signal continues for 8 times, the mode is automatically changed to CLV-S mode. When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is perfomred in register E. The description of these registers are detialed in **"CPU interface"**.

Note: When PSSL = "L", DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

8) CLV-A' : Register E = 0101'B

New auto servo mode added to the CX23035. The difference between CLV-A. and CLV-A is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.

The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

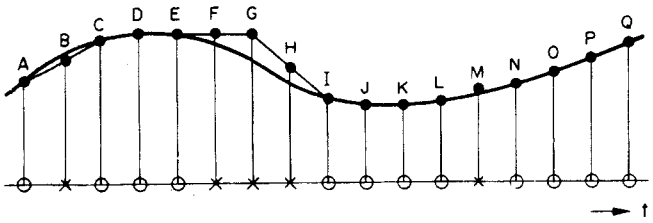
CIRCUIT DESCRIPTION

• Interpolation and D/A converter interface

1) Interpolation circuit block

3 byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8 bits and more significant 8 bits. The total 16 bits constitute the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16 bit data. Therefore, data with C2 pointer is subject to interpolation in this block.



O : Without C2 pointer
X : With C2 pointer

Mean value interpolation

$$B = \frac{1}{2}(A+C)$$

$$H = \frac{1}{2}(E+I)$$: When pointers are continuous

$$M = \frac{1}{2}(L+N)$$

Previous value hold

$$F = G = E$$

16 bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H". C2PO signal outputs C2 pointer to the 16 bit data directed to DA01–DA16 (PSSL = H), DA16 (PSSL = L). In other words, it means that the 16 bit data that is output when C2PO is "H" is interpolated data.

2) Explanation of muting and attenuator

In the muting block it is possible to mute (– ∞ dB) or attenuate (–12dB) the audio signal in accordance with the MUTG terminal and ATTM signal of the CPU interface block.

ATTM	MUTG	Attenuation value	Remarks
0	0	0dB	
1	0	–12dB	
0	1	– ∞ dB	See Note
1	1	–12dB	See Note

NOTE : When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.
Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter is loaded.

CIRCUIT DESCRIPTION

- **Mode setting**

The various kinds of mode can be set by combining the following pins. (Refer to the table below.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.

MD2 pin : Mainly for selection of the digital out function.

MD3 pin : Mainly for selection of the digital filter function.

PSSL pin : Mainly for selection between serial and parallel output.

SLOB pin : Selection between offset binary and 2's complement.

Input terminal					Function					(Note)	Compatible IC	
MD1	MD2	MD3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	CD ROM/AUDIO	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Seri	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
L	H	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	L	L	L	L	8M	↓	DF ON	Seri	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
H	L	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	H	H	L	L	16M	DO ON	↓	Seri	2's	CD ROM	○	
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

(Note)

- 8M/16M : Selection of clock, XTAL or XTAO. 8.4672MHz/16.9344MHz
- DO OFF/ON : Digital out OFF/ON
- DF OFF/ON : Digital filter OFF/ON
- P/S : Parallel output/serial output
- OB/2's : Offset binary/2's complement
- CD ROM/AUDIO : Compatible to CD ROM/Compatible to audio

1) Selection of clock

The oscillator clock for XTAI and XTAO is available at 16.9344MHz and 8.4672MHz. However, when digital out is used, the clock must be set to 16.9344MHz.

2) Selection of digital out (Refer to "D/A interface")

When digital out is set to ON, a signal conforming to the D/A interface format is output from the DOTX pin. When it is set to OFF, the DCTX pin outputs the WFCK signal. In the DP-969, this function is fixed to ON.

3) Selection of digital filter

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

4) Selection of parallel output/serial output

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data. When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

DA01 → C1F1 : } Error correction status monitor
DA02 → C1F2 : } output at C1 decode.
DA03 → C2F1 : } Error correction status monitor
DA04 → C2F2 : } output at C2 decode.
DA05 → C2FL : Correction status output, C2FL = C2F1·C2F2.
DA06 → C2PO : C2 pointer signal.
DA07 → RFCK : Read frame clock signal, 7.35kHz when locked to the crystal line.
DA08 → WFCK : Write frame clock signal, 7.35kHz when locked.
DA09 → $\overline{\text{PLCK}}$: 1/2 of the divided signal from the VCO pin, 4.3218MHz when locked.
DA10 → UGFS : Non-protect frame sync signal.
DA11 → GTOP : Frame sync protect status display signal.
DA12 → RAOV : Jitter margin over or underflow display signal.
DA13 → C4LR : 4 times the LRCK signal.
DA14 → $\overline{\text{C21O}}$: Bit clock (invert signal of C21O).
DA15 → C21O : Internal system clock (4.2336MHz when DF is ON, 2.1168MHz when CXD1125Q or DF is OFF).
DA16 → DATA : Serial data output (MSB or LSB first output).

CIRCUIT DESCRIPTION

5) Selection of OFFSET BINARY/2'S COMPLEMENT

When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

6) Selection of.CD ROM/AUDIO compatibility

When MD1 = MD2 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8 bits of the 16 bits, only the C2 pointer corresponding to the upper 8 bits goes "H", and the lower 8 bits are processed as the correct data.

- **D/A Interface**

The player incorporates a D/A interface output (digital output) and the digital signal is output from the DOTX pin. The digital signal is output after passing through interpolation, mute and attenuator circuits. The 4 control bits (ID0, ID1, COPY, EMPHASIS) in the C-bit channel status perform a CRC check and are revised only when it's OK.

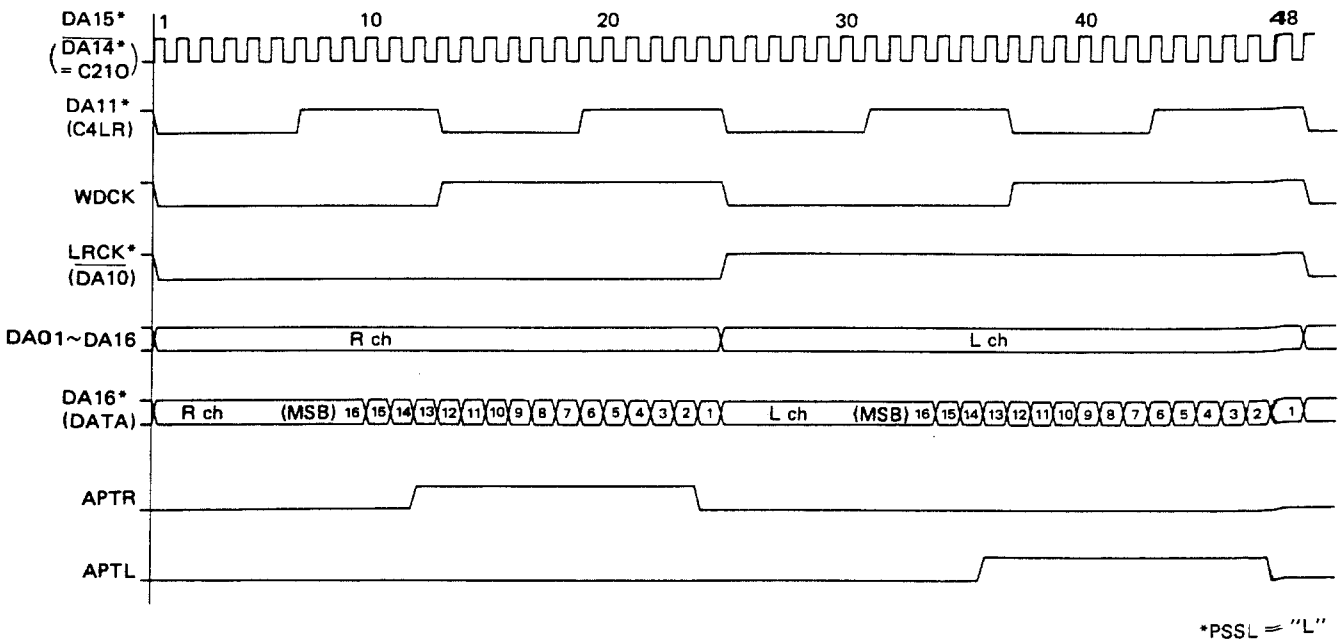
- **Countermeasures to defect**

To counter a defect, the PDC pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after approx. 0.55ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".

The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK pin. After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".

This operation is similar to that for the FSW pin. However, while the FSW outputs a fixed signal when not in CLV-A' mode, the LOCK pin always output the above signal.

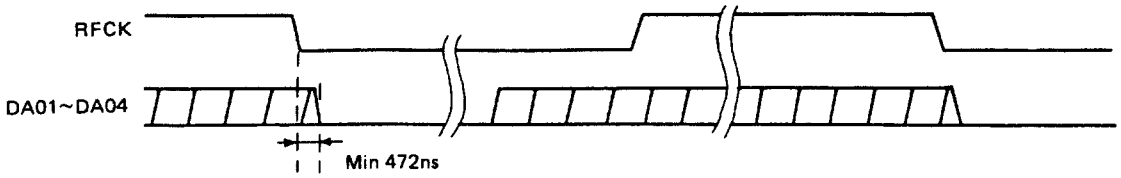
- **Timing chart**



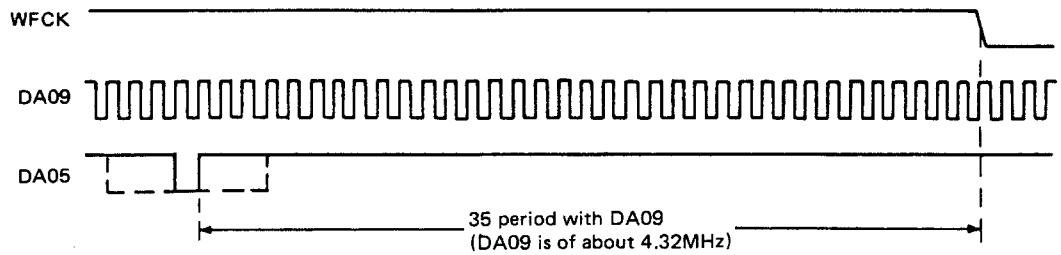
*PSSL = "L"

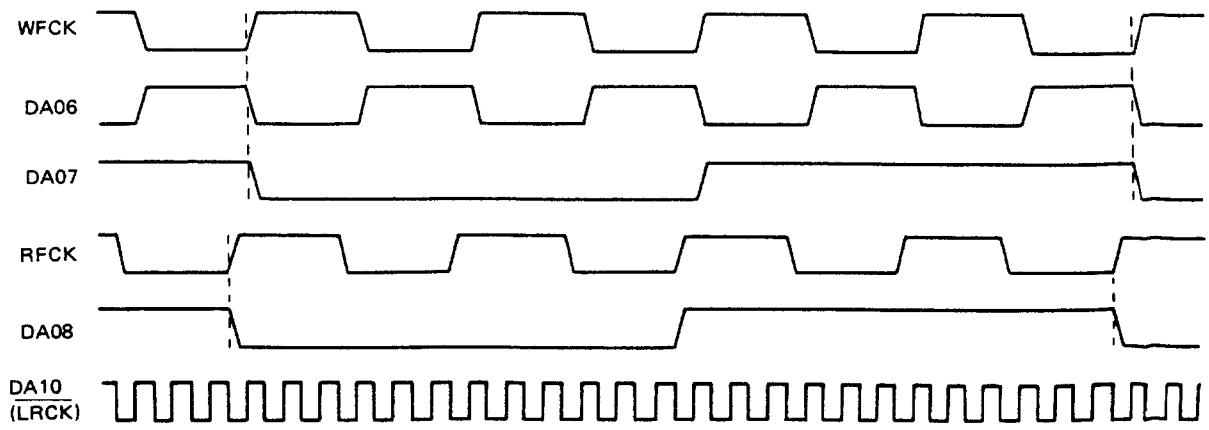
Timing chart of audio output

CIRCUIT DESCRIPTION



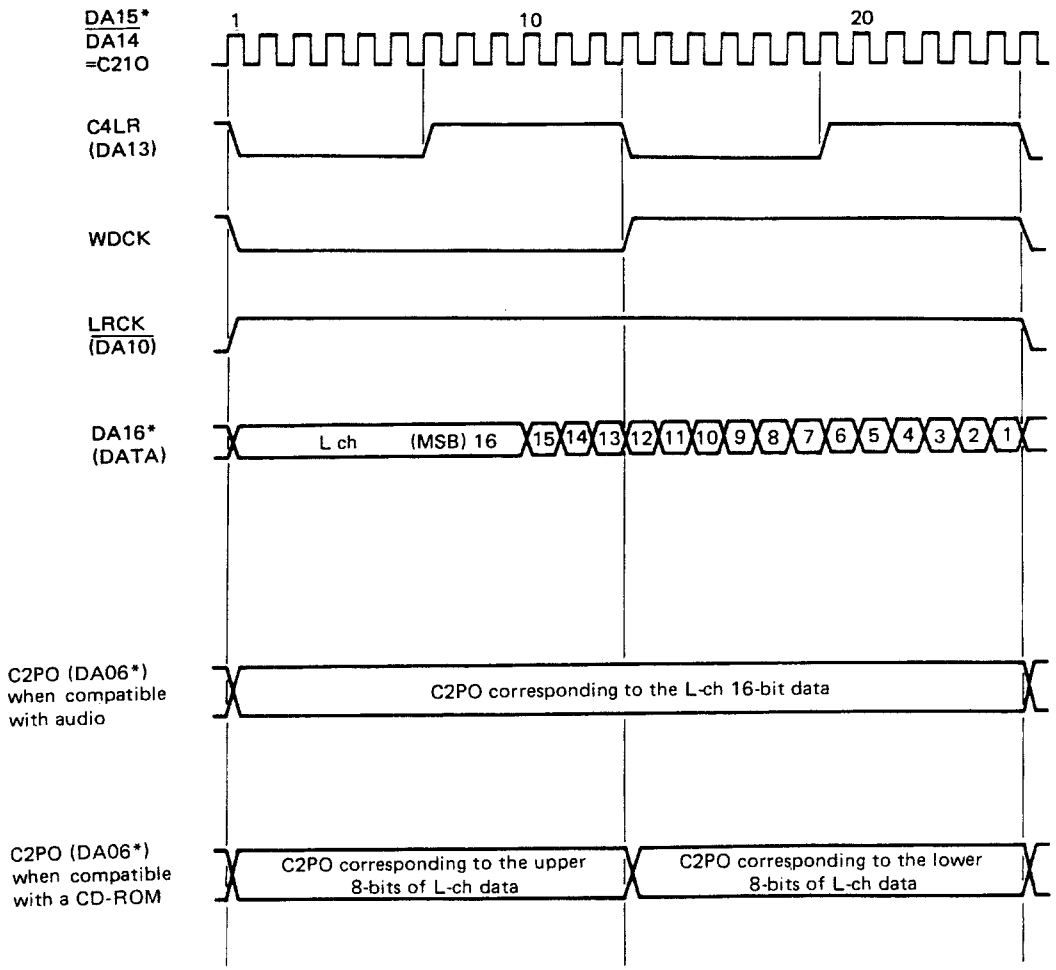
* DA01~DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
* ANDing signal of C2F1 and C2F2 is output out of C2FL termnal.





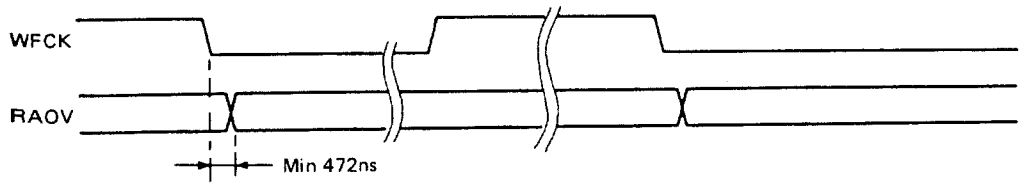
Timing chart of DA01 ~ DA16 output when PSSL = "L"

CIRCUIT DESCRIPTION



Timing chart of C2PO output (when PSSL = "L")

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

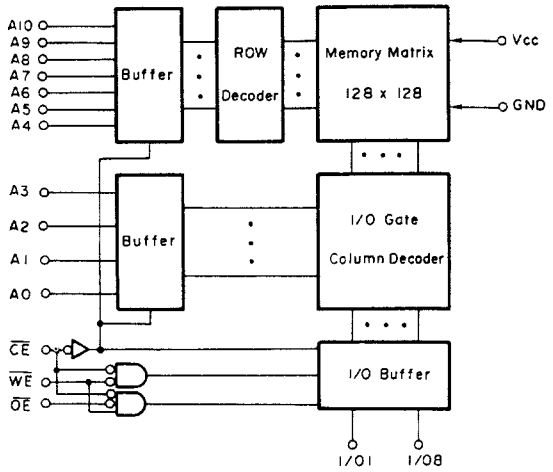


Timing chart of RAOV output

CIRCUIT DESCRIPTION

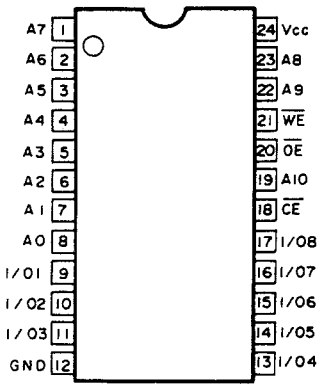
IC15: CXK5816SP-12 (X25-3120-11) Static RAM

Block diagram



Pin arrangement

(Top View)

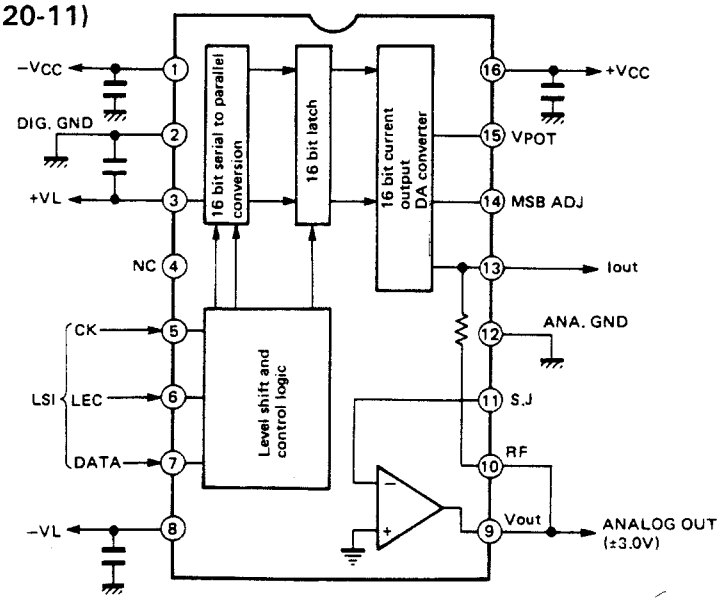


Pin description

Pin symbol	Pin function
A0 ~ A10	Address input
I/O1 ~ I/O8	Data in/out
CW	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+ 5 V power supply
GND	Ground

IC10, 11: PCM56P-K (X25-3120-11) D/A Converter

Block diagram/ Terminal connection diagram

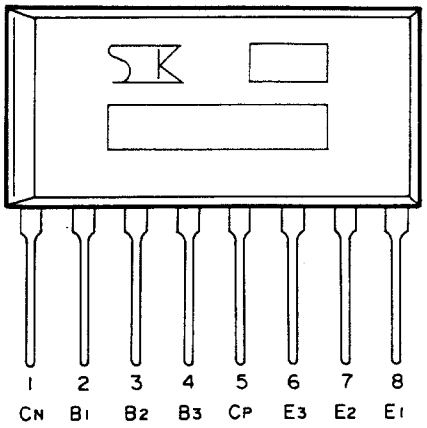


Explanation of terminals

Terminal No.	Terminal name	Function	Terminal No.	Terminal name	Function
1	–Vcc	Analog negative power supply.	9	Vout	Voltage output
2	DIG GND	Digital ground.	10	RF	Feedback resistor.
3	+ VL	Logic positive power supply.	11	S.J	Summing junction (op amp. input).
4	NC	No connection.	12	ANA GND	Analog ground.
5	CK	Clock input.	13	Iout	Current output.
6	LEC	Latch enable control input.	14	MSB ADJ	MSB adjustment terminal.
7	DATA	Data input.	15	V POT	Potentiometer terminal.
8	–VL	Logic negative power supply	16	+ Vcc	Analog positive power supply.

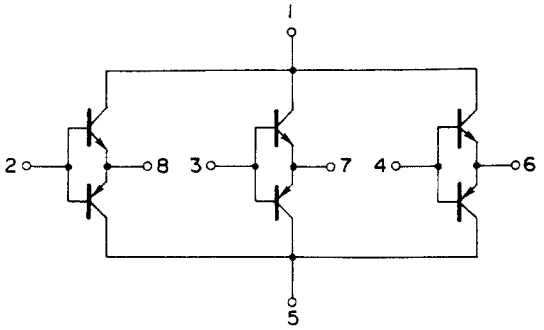
CIRCUIT DESCRIPTION

Q25: STA341M (X25-3120-11)
Transistor array



E: Emitter
B: Base
C: Collector

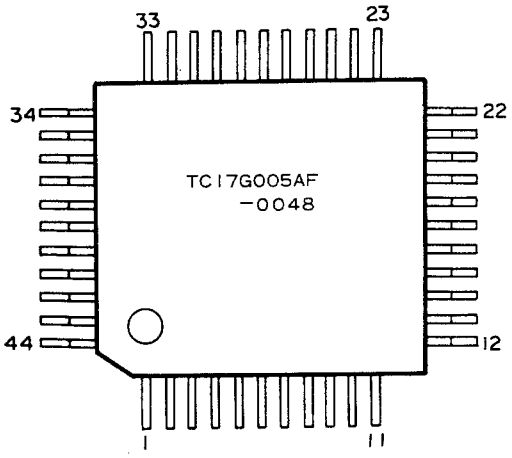
Equivalent circuit



IC12: TC17G005AF-0048 (X25-3120-11)
D/A Distortion compensator

Pin arrangement (Top view)

(Top View)



Pin description

Pin No.	Symbol	I/O	Pin function
1	CKL	O	L-channel clock output
4	Vss	—	GND (Ground)
5	CKR	O	R-channel clock output
7	LRD	O	Latch enable control output
8	Vss	—	GND (Ground)
12	CKI	O	System clock for external IC
14	Xo	O	Crystal pin for clock oscillation (16.934 MHz)
15	XI	I	Crystal pin for clock oscillation (16.934 MHz)
17	VDD	—	+5 V power supply
28	Vss	—	GND (Ground)
39	VDD	—	+5 V power supply
40	LR	I	LRCK input (4 fs)
41	BCK	I	BCK input (4 fs)

MECHANISM DESCRIPTION

Mechanism operation description

Fig. 1 shows the mechanism positioning in the STOP mode. The OPEN/CLOSE operation when loading the disc is described below.

Note :

In the operation description, the black and white arrows shows the following code :

Black arrow : Shows the opening direction of the tray (Tray OPEN).

White arrow : Shows the closing direction of the tray (Tray CLOSE).

Also in the operation description and illustrations, numbers in brackets ( ) followed by the part name show the identifying numbers of the disassembly diagram in the Service Manual.

1. OPEN/CLOSE operation

The center of the OPEN/CLOSE lug detection leaf switch installed on the PC board (J25-4904-02(A/3)) on the rear of the mechanism is pressed to the right by lower side of the tip of the black switch arm (6) installed on the slider ass'y (11) when the tray is closed, and the information is transferred to the microprocessor. This status is called the tray CLOSE operation. The operation from this status to the condition when the tray is completely opened by pressing the OPEN/CLOSE key is described.

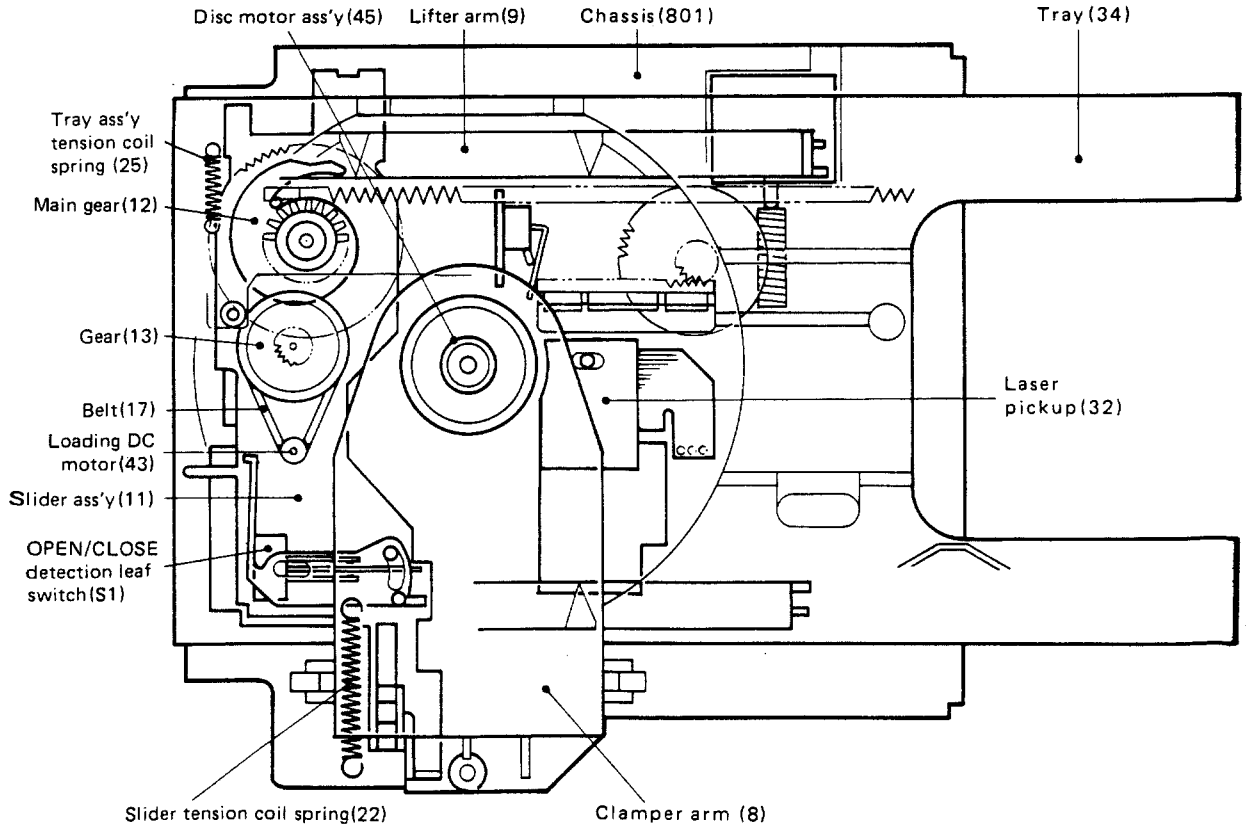


Fig. 1 Tray closed status

MECHANISM DESCRIPTION

As shown in Fig. 2, loading DC motor (43) rotates in the direction of the black arrow ❶ and transfers the rotation of the black arrow ❷ to the gear (13) via the belt (17), and also rotates the main gear (12) in the direction of the black arrow ❸ with the lower gear section of the gear (13). The main gear (12) contains the cam on its upper surface. Along with the surface of the cam, protrusion A located in the lower side of the slider ass'y (11) is shifted and the slider ass'y (11) begins to move in the direction of the black arrow ❹.

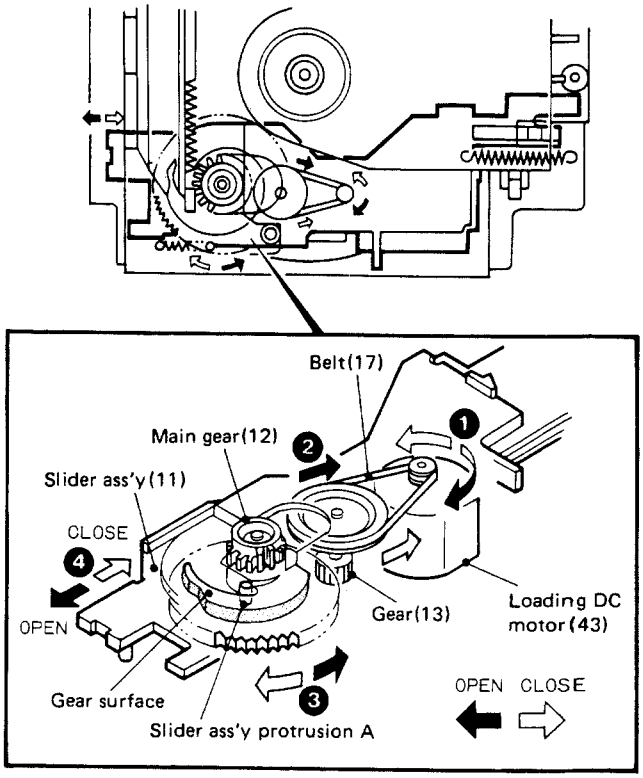


Fig. 2 Loading motor rotation transmission

Fig. 3 shows the movement of protrusion A of the slider ass'y(11) in the direction of the black arrow ❹ until the tray is completely opened.

The slider ass'y(11) releases the OPEN/CLOSE detection leaf switch(S1) from the CLOSE condition and pulls the foot section of the clamper arm(8) in the direction of the black arrow ❹ by the groove section of the slider ass'y(11). By this, the clamper arm(8) is lifted in the direction of the black arrow ❻ with a support as a center to the disc release condition from the disc clamping condition.

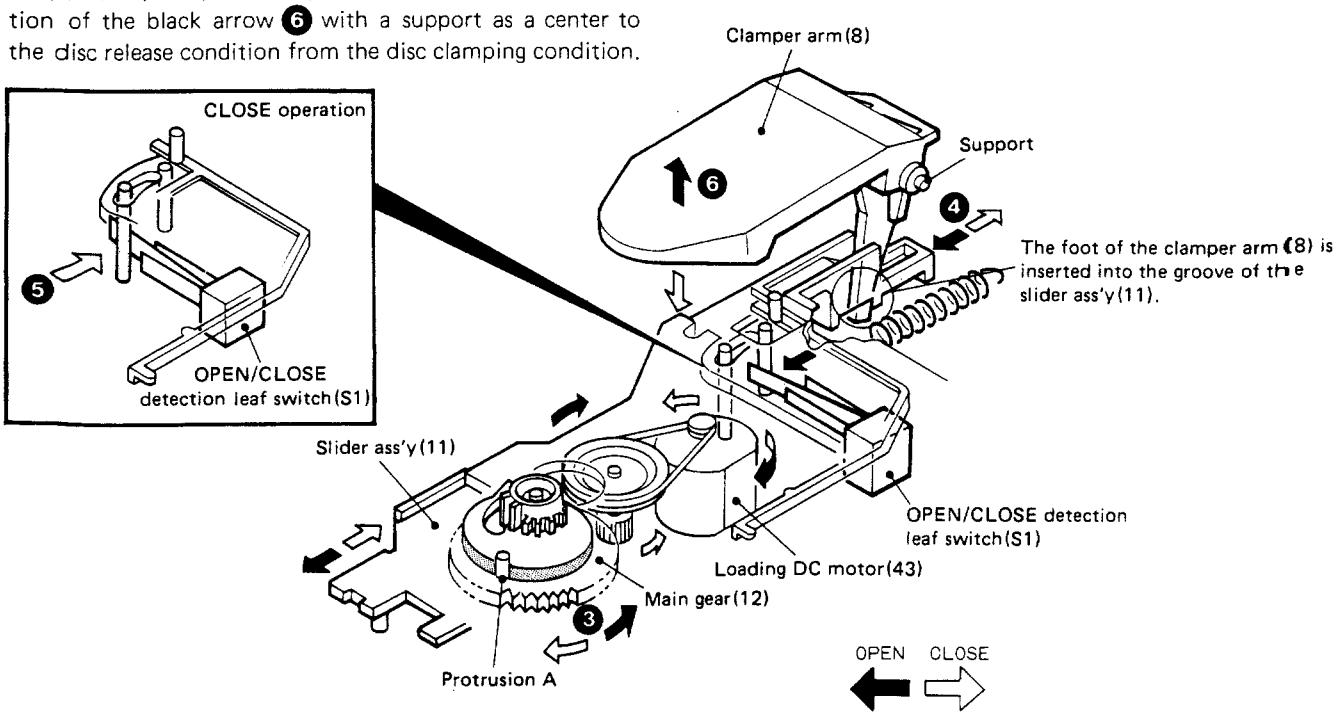


Fig. 3 Clamper arm operation

MECHANISM DESCRIPTION

Fig. 4 shows the condition when the tray is completely opened. The tray is "sloped" as shown in the figure. When the tray moves in the direction of the black arrow ❺ OPEN direction, the white protrusion climbs the "slope" to short the OPEN/CLOSE detection leaf switch(S1) in the reverse direction of the STOP condition, then informs the microprocessor that the OPEN operation has completed and to stop the rotation of the loading DC motor(43).

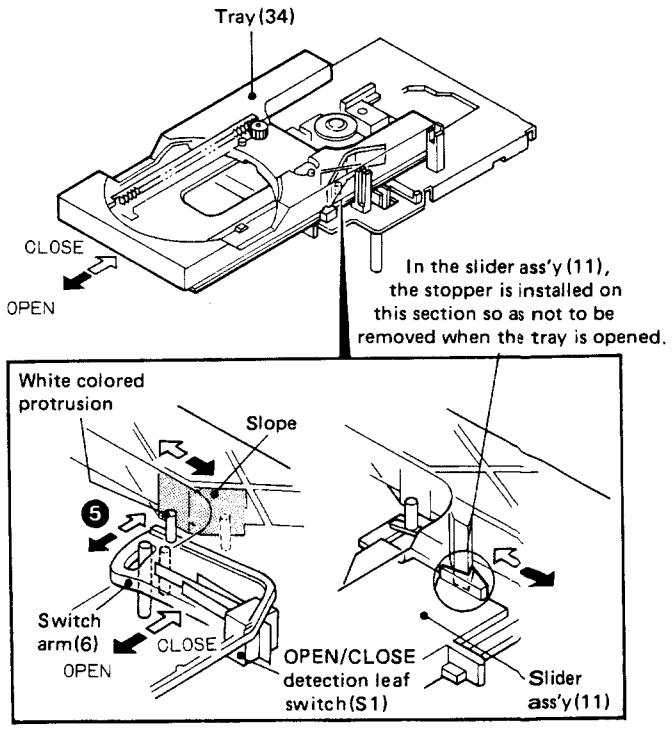


Fig. 4 Each limit switch when opening/closing the tray

Fig. 5 shows the OPEN operation until the disc is lifted from the turntable and placed on the disc tray so that the disc is removed from the player. These operations are performed almost at the same time as the up operations of the clamper arm(8) when the tray is opened as described in Fig. 2 to 4 above.

The tray(34) incorporates the lifter arm(9) which is required to support the disc when the tray is opened/closed and the lifter slider(10) which drives the lifter.

When the tray is opened, the slider ass'y(11) is shifted in the direction of the black arrow ❹ In the slider ass'y, lug a is installed to slide the lifter slider horizontally (toward the left and right). And the lifter slider(10) is always pulled in the direction of the black arrow ❼ by the tray ass'y tension coil spring(25).

For this, when the slider ass'y(11) is moved to the OPEN direction (in the direction of the black arrow ❹), the lifter slider(10) is also shifted to the left by the lug a. The lifter slider(10) has grooves on its left and right ends to lift the lifter arm up/down.

In the OPEN operation, when the lifter slider(10) is moved in the direction of the black arrow ❼, protrusion B of the lifter arm(9) is slide in the groove using the support as a center, and the lifter arm is lifted in the direction of the black arrow ❽.

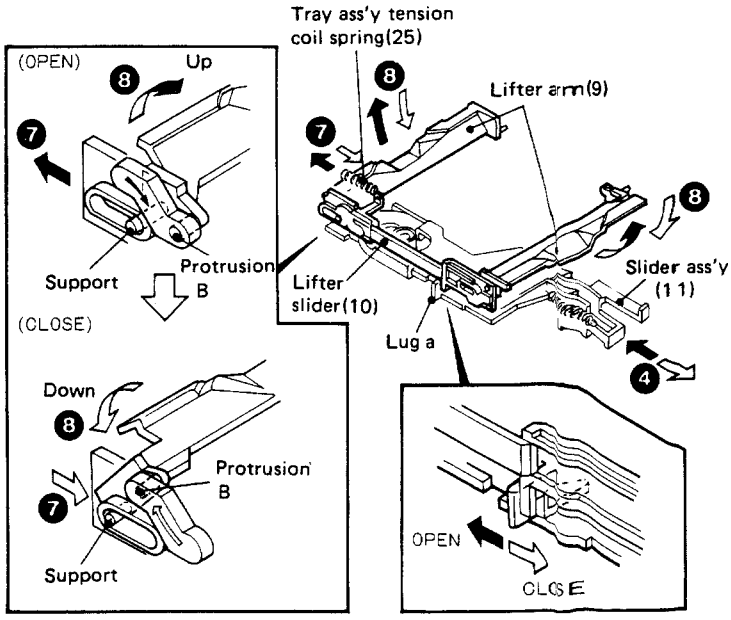


Fig. 5 Lifter arm up/down operation

MECHANISM DESCRIPTION

Fig. 6 shows the operation of the main gear(12) which actually performs the OPEN/CLOSE operation of the tray described above.

In the upper surface of the main gear(12), there's a gear to open or close the tray. Among the gear teeth, only two teeth are longer than the other, for triggering the OPEN operation.

First these longer teeth trigger the OPEN operation, then the whole gear engages the gear rack of the surface of the tray to initiate the OPEN operation.

At this time, protrusion A installed on the lower side of the slider ass'y(11) is located at the position where the main gear(12) is rotated approx. 360 degree from the STOP position. At this position, when the triggering gear and the gear rack of the tray are engaged to initiate the OPEN operation, protrusion A will drop to the STOP position again from the convex of the main gear(12) cam surface. To prevent this, the white colored roller installed on the slider ass'y(11) releases protrusion A from the cam surface of the main gear(12), so as not to contact with the cam surface while the main gear(12) is engaged with the gear rack on the back of the tray in OPEN/CLOSE operation.

Since this roller is always pulled in the right direction (viewd from the front) by the slider tension coil spring(22) and the arm pressure coil spring(24), it slides while pressing the guide surface on the back of the tray in the right direction in the tray OPEN/CLOSE operation.

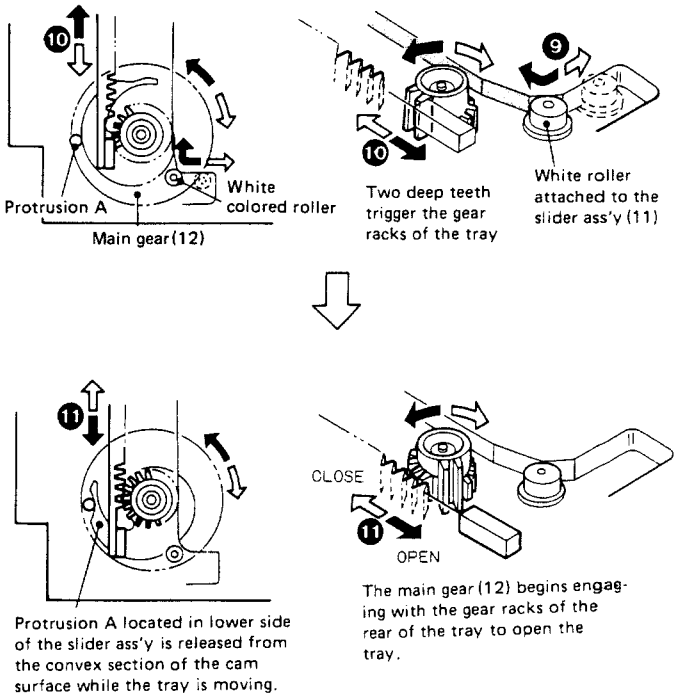


Fig. 6 Gear (12) operations

2. Disassembling procedure of mechanism section

2–1. Removing the clamper arm

1) While lightly pressing the clamper arm from the top ❶, remove the fixing lugs on both sides in the direction of arrows ❷ and ❸.
2) Remove the clamper arm in the direction of arrow ❹

Note : Be sure to remove the fixing lugs on both sides of the clamper arm while pressing the clamper arm in the direction of arrow ❶. Since the lugs are solid, if forcibly performed, they might be broken.

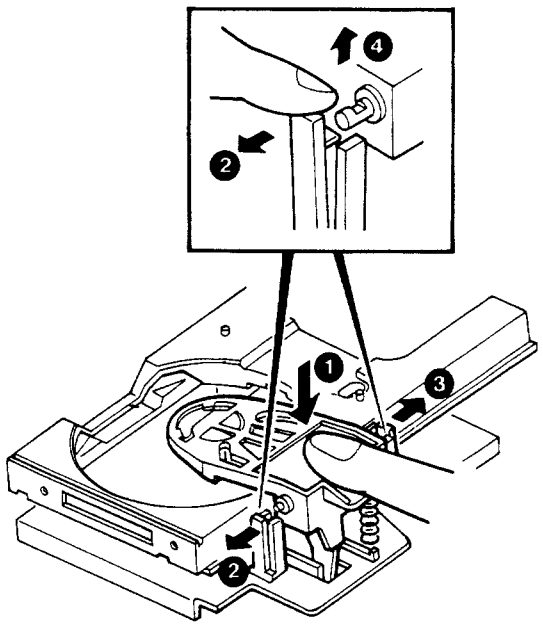


Fig. 1 Removing the clamper arm

MECHANISM DESCRIPTION

2—2. Attaching the clamper arm

1) Insert the foot section of the clamper arm into the groove of the slider ass'y (❺).
2) At this time confrim that portrusion A of the clamper arm is inserted into the center of the arm pressure coil spring.
3) Put the support of the clamper arm to the lug section of the outsert of the mechanism by pressing from the top (❻).

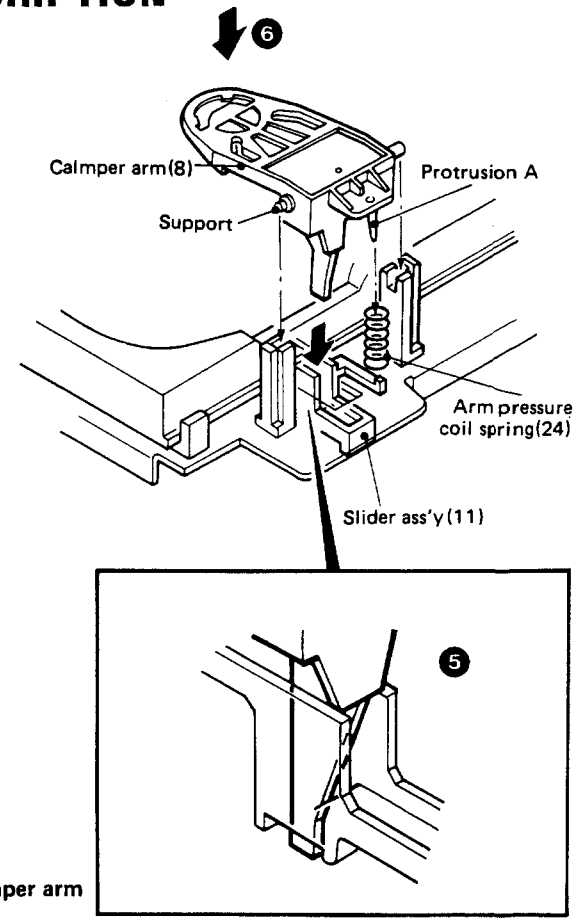


Fig. 2 Attaching the clamper arm

2—3. Removing the tray

1) While pressing the hook section of the slider ass'y in the direction of arrow ❼ , pull out the tray in the direction of arrow ❽ to remove it (❾).

Note : Be sure not to release your finger when pressing the hook. If the hook is released, the stopper on the upper surface of the slider ass'y will come in contact with the stopper of the tray and the tray will not be removed.

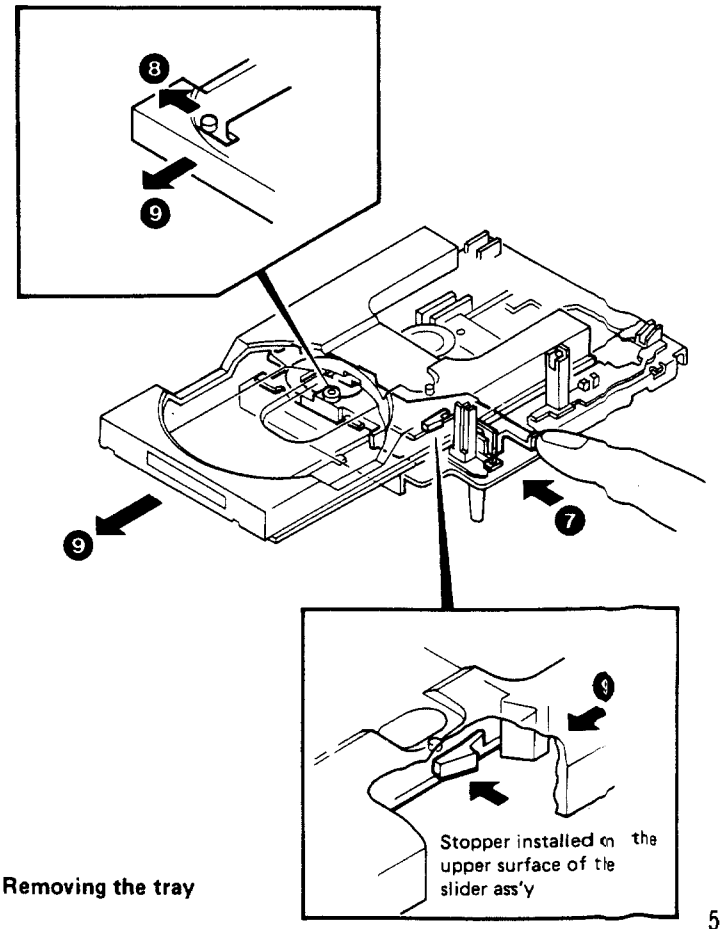


Fig. 3 Removing the tray

MECHANISM DESCRIPTION

2–4. Attaching the tray

1) Attach the collars firmly on both sides of the tray to the four section supporting and guiding the tray as shown in the Fig. 4.
   First attach the front two section then attach the rear two sections as shown in ⑩.

Note : The gear offset of the mechanism after removing/ attaching the tray will be reset automatically by performing the OPEN/CLOSE operation

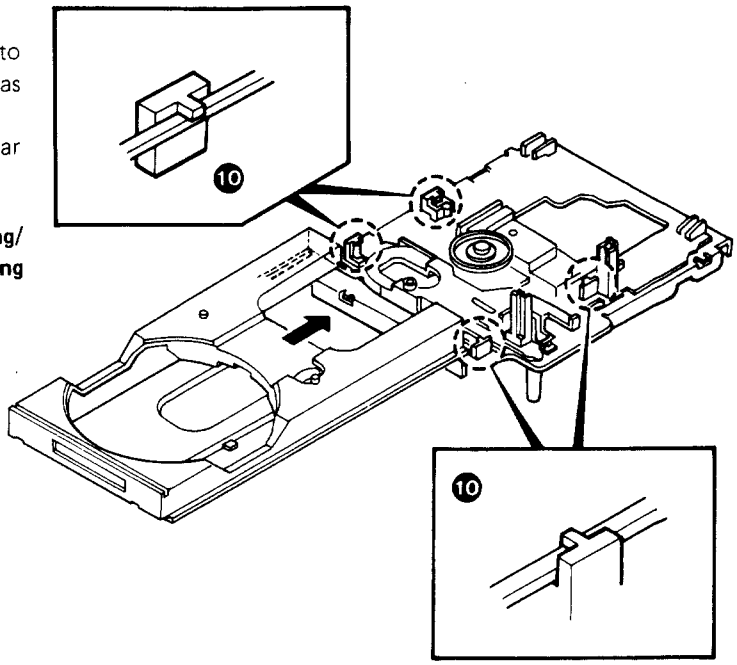


Fig. 4 Attaching the tray

2–5. Removing the slider ass'y

1) Removing the slider tension coil spring attached to the slider ass'y (⑪).
2) Slide the slider ass'y in the direction of arrow ⑫ until it reaches the position where it can be removed from the outsert section supporting the slider ass'y.
3) Remove the slider ass'y by pulling out right above in the direction of arrow ⑬ .

Note : If the slider ass'y is removed askew, the OPEN/ CLOSE detection leaf switch on the back of the tray might be bent down.

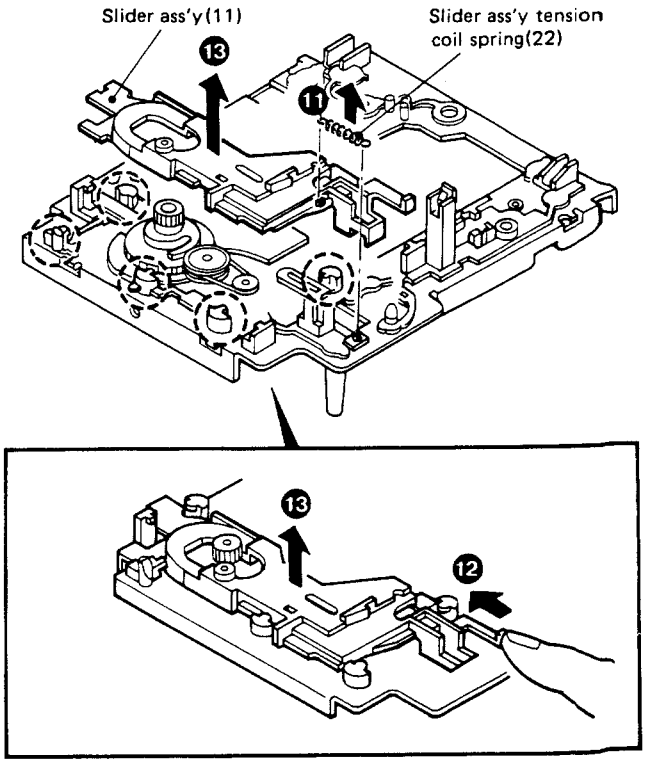


Fig. 5 Removing the slider ass'y

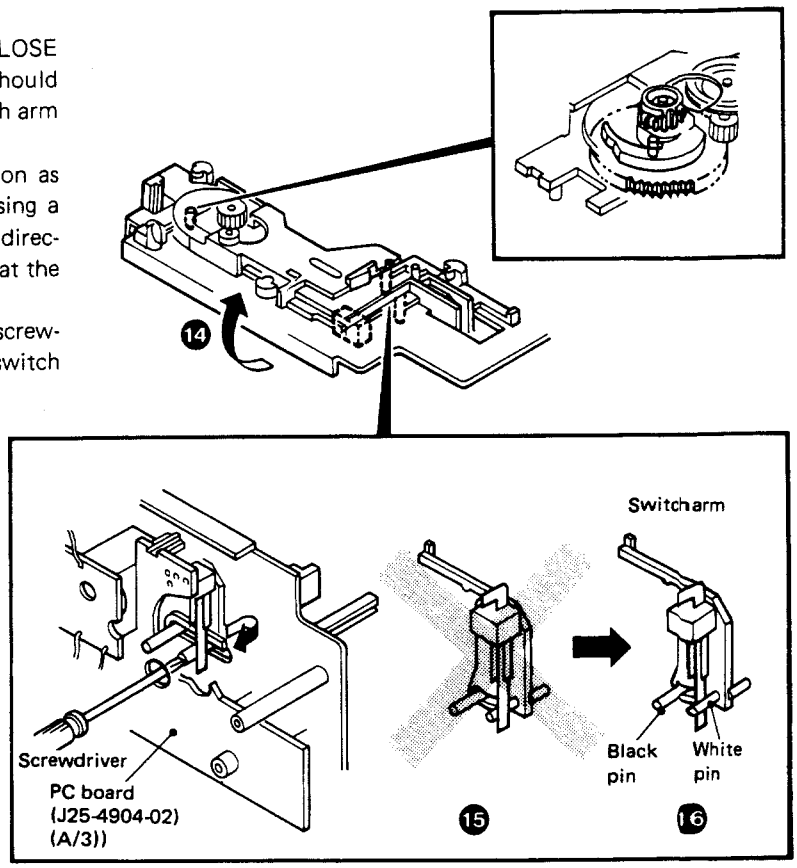
MECHANISM DESCRIPTION

2—6. Attaching the slider ass'y

The long metal piece at the center of the OPEN/CLOSE detection leaf switch on the rear of the mechanism should be set between the white and black pins of the switch arm installed on the rear of the slider ass'y.

If it is inserted simply, it will be set the position as shown in ⓯. At this time, correct the position using a screwdriver by lifting the slider ass'y slightly in the direction ⓮ so that the white pin of the switch arm is set at the position as shown in ⓰.

A round hole is on the PC board for inserting the screwdriver. This is used for correcting/checking the switch position when working.



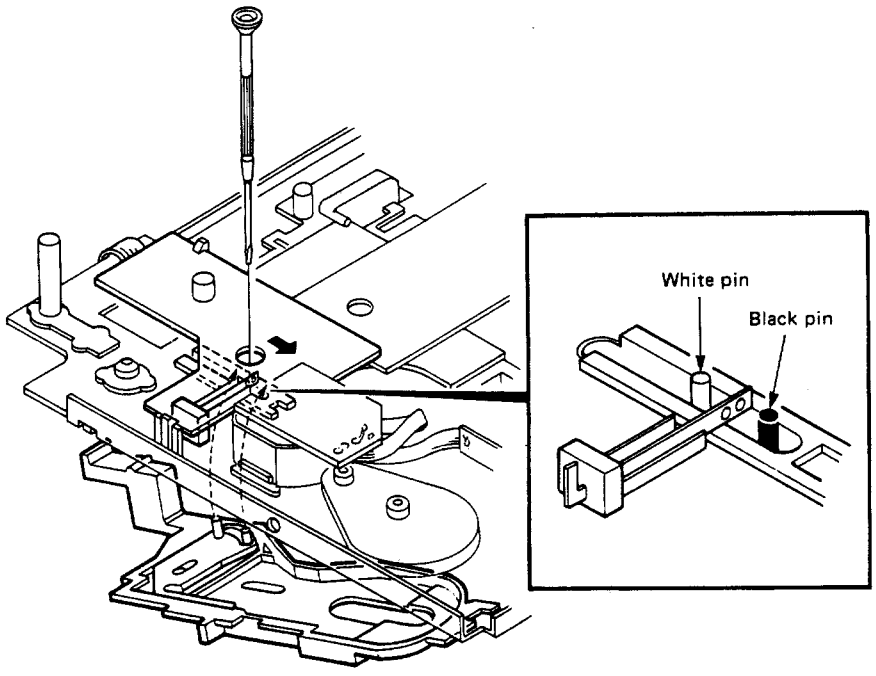


Fig. 6 Attaching the slider ass'y

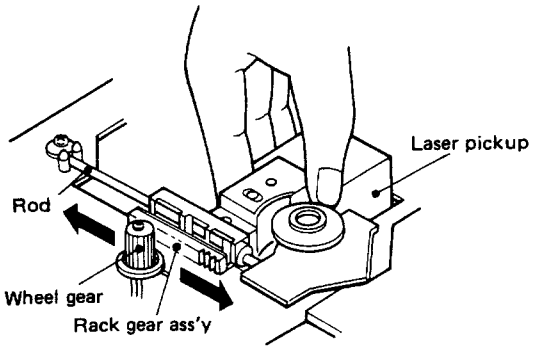
MECHANISM DESCRIPTION

2—7. When moving the pickup forcibly

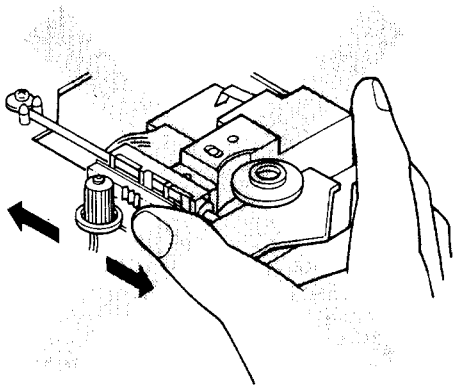
Do not move the rack gear ass'y by hand as shown in Fig. (B). The clearance between the wheel gear and the rack gear ass'y might be changed if bent.

When moving the pickup on repair, hold the main body of the pickup with the section as close to the rod as possible, then move it forcibly. (Fig. A).

Note : Do not move the pickup forcibly unless required.



(A)



(B)

Fig. 7 Pickup gear movement

ADJUSTMENT

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	LASER POWER	–	Apply the sensor section of the optical power meter on the pickup lens.	Short-circuit pins TEST and turn power on to enter the Test mode. Press the +10 key, the tray opens and the LD emits light.	VR101 ALPC circuit VR installed on the pickup	0.1mW	(a)
2	LASER PICKUP OPERATING CURRENT (Only when the pickup seems defective.)	–	Connect a DC ammeter across CN2 pin 6 and the pattern. (X25-3120)	Short-circuit pins TEST and turn power on to enter the Test mode. Press the +10 key, the tray opens and the LD emits light.	–	+5.5mA current value labeld on the laser pickup. If current is 40mA or more over the above value, it's defective.	(b)
3	VCO	–	Connect a frequency counter to TP10(PLCK) (X25-3120)	Turn Power OFF, then ON again. Stop mode	L13 (X25-3120)	4.32MHz	(c)
4	FOCUS ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF CH2: TE (X25-3120)	PLAY	FE BALANCE VR4 (X25-3120)	Optimum eye pattern	(d)
5	TANGENTIAL	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF CH2: TE (X25-3120)	PLAY	Screw on right side of mechanism	Optimum eye pattern	(d)
6	DIFFRACTION GRATING (1)	Test disk Type 4	Connect an oscilloscope as follows. CH1: RE CH2: TE (X25-3120)	Enter the test mode by turning Power ON while shorting the Test Pin. Press the CHECK Key and confirm that the display is " 03oo ".	Adjusting hole in the lower side of the laser pickup.	Maximum amplitude (See Photos 1 and 2.)	(d)
7	DIFFRACTION GRATING (2) " Polarity check "	Test disk Type 4	Connect an oscilloscope as follows. CH1: RE CH2: TE (X25-3120)	Press the CLEAR key and turn the tracking servo ON. Confirm that the display is " 04oo ".	Adjusting hole in the lower side of the laser pickup.	Confirm that the eye pattern is presented correctly.	(d)
8	DIFFRACTION GRATING (3)	Test disk Type 4	Connect an oscilloscope as follows. CH1: RE CH2: SSPT (X25-3120)	Press the PLAY key, and confirm that the display is " 05oo ".	Adjusting hole in the lower side of the laser pickup.	Check that they are as Photo 3. *Photo 4 shows the defective example.	(e)
9	TRACKING ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RE CH2: TE (X25-3120)	Press the CHECK key, and confirm that the display is " 03oo ".	TE.BALANCE VR3 (X25-3120)	Symmetry between upper and lower patterns, or DC=0±0.05V	(d)
10	FOCUS GAIN	Test disc Type 4 Apply 900Hz, 50mVrms signal to CN4 pin 2 of PC board X25-3120	Use a servo jig, or connect a 47kΩ, 470pF LPF to pin 1 of CN4. (X25-3120)	Turn Power OFF then ON again, and press the PLAY key.	FOCUS GAIN VR5 (X25-3120)	50mVrms	(f)
11	TRACKING GAIN	Test disc Type 4 Apply 900Hz, 50mVrms signal to CN4 pin 4 of PC board X25-3120	Use a servo jig, or connect a 47kΩ, 470pF LPF to pin 5 of CN4. (X25-3120)	PLAY	TRACKING GAIN VR6 (X25-3120)	50mVrms	(g)
12	DAC OUTPUT	Test disk Type 4	Connect an AC voltmeter to the output terminal(FIXED).	Play the 1kHz, 0dB signal in track No.2.	VR1: L VR2: R (X25-3120)	1.9~2.0Vrms	(h)

(Note)Type 4 disk: SONY YEDS-18 Test Disk or equivalent.

REGLAGES

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LECTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
1	PUISSANCE LASER	–	Appliquer la section détecteur du compteur de puissance optique sur la lentille du capteur.	Court-circuiter les broches TEST et mettre sous tension pour passer dans le mode d'essai. Appuyer sur la touche +10, le plateau s'ouvre et le LD émet de la lumière.	VR101 VR de circuit ALPC installé sur le capteur	0.1mW	(a)
2	Courant de fonctionnement du capteur laser (Uniquement quand le capteur semble défectif.)	–	Raccorder un ampèremètre CC en travers de la broche 6 de CN2 et la forme. (X25-3120)	Court-circuiter les broches TEST et mettre sous tension pour passer dans le mode d'essai. Appuyer sur la touche +10, le plateau s'ouvre et le LD émet de la lumière.	–	+5.5mA de valeur de courant indiquée sur le capteur laser. Si le courant est de 40mA ou bien supérieur à la valeur ci-dessus, il est défectif.	(b)
3	VCO	–	Raccorder un compteur de fréquence à TP10(PLCK). (X25-3120)	Couper l'alimentation, puis la redonner. Mode d'arrêt	L13 (X25-3120)	4.32MHz	(c)
4	BALANCE D'ERREUR DE MISE AU POINT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1:RF CH2:TE (X25-3120)	PLAY	FE BALANCE VR4 (X25-3120)	Forme optimum	(d)
5	TANGENTIEL	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1:RF CH2:TE (X25-3120)	PLAY	Vis sur le côté droite du mécanisme	Forme optimum	(d)
6	RESEAU DE DIFFRACTION (1)	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1:RF CH2:TE (X25-3120)	Entrer en mode de test en mettant l'alimentation en circuit tout en court-circuitant la broche test. Presser la touche CHECK et s'assurer que l'affichage est " 03oo ".	Trou d'ajustment dans le côté inférieur du capteur laser	Amplitude maximum (voir le photos 1 et 2).	(d)
7	RESEAU DE DIFFRACTION (2) " Vérification de polarité "	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1:RF CH2:TE (X25-3120)	Presser la touche CLEAR et mettre l'asservissement d'alignement en circuit. S'assurer que l'affichage est " 04oo ".	Trou d'ajustement dans le côté inférieur du capteur laser	S'assurer que la forme se présente correctement.	(d)
8	RESEAU DE DIFFRACTION (3)	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1:RF CH2:SSPT (X25-3120)	Presser la touche PLAY et s'assurer que l'affichage est " 05oo ".	Trou d'ajustement dans le côté inférieur du capteur laser	Vérieur qu'ils sont comme dans la photo 3. *La photo 4 montre un exemple défectif.	(e)
9	BALANCE D'ERREUR D'ALIGNEMENT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1:RF CH2:TE (X25-3120)	Presser la touche CHECK et s'assurer que l'affichage est " 03oo ".	TE BALANCE VR3 (X25-3120)	Symétrie entre les formes supérieure et inférieure ou DC=0±0.05V	(d)
10	GAIN DE MISE AU POINT	Disque test Type 4 Appliguer un signal 900Hz, 50mVrms à la troche 2 de CN4 sur la plaquette X25-3120.	Utiliser un gabarit d'asservissement ou raccorder un FPH de 47kΩ, 470pF la troche 1 de CN4.	Couper l'alimentation et la redonner puis presser la touch PLAY.	GAIN DE MISE AU POINT VR5 (X25-3120)	50mVrms	(f)
11	GAIN D'ALIGNEMENT	Disque test Type 4 Appliguer un signal 900Hz, 50mVrms à la troche 4 de CN4 sur la plaquette X25-3120.	Utiliser un gabarit d'asservissement ou raccorder un FPH de 47kΩ, 470pF la troche 5 de CN4.	PLAY	GAIN D'ALIGNEMENT VR6 (X25-3120)	50mVrms	(g)
12	SORTIE DAC	Disque test Type 4	Raccorder un voltmètre CA sur la borne de sortie (FIXED).	Lire le signal 1kHz, 0dB dans la piste n° 2.	VR1:G VR2:D (X25-3120)	1.9~2.0Vrms	(h)

(Remarque)Disque de type 4:Disque test SONY YEDS-18 ou équivalent.

ABGLEICH

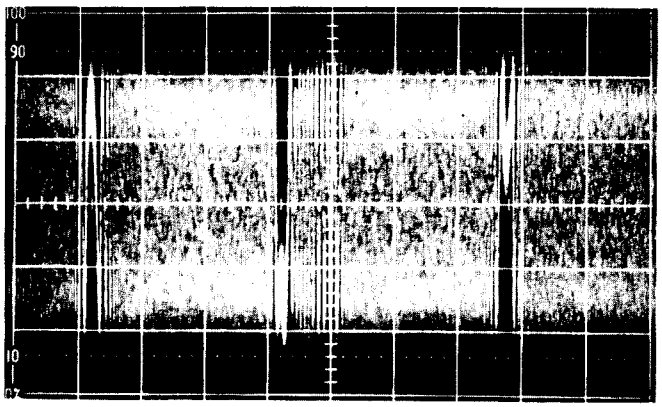
NR.	GEGENSTAND	EINGANGS-EINSTELLUN	AUSGANGS-EINSTELLUNGE	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB.
1	LASERLEISTUNG	–	Das Sensorteil des optischen Leistungmeters auf die Aufnehmerlinse ansetzen.	Die Stifte TEST kurzschließen und die Spannungsversorgung einschalten, um den Test-Modus zu aktivieren. Die Taste +10 drücken, dann öffnet sich der Träger, und die LD gibt Licht aus.	VR101 Regelwiderstand des ALPC-Schaltkreises am Tonabnehmer	0,1mW	(a)
2	BETRIEBSSTROM DES LASERTONABNEHMERS (Nur wenn der Tonabnehmer defekt zu sein scheint)	–	Ein-Gleichstrom-Amperemeter zwischen CN2 Stift 6 und dem Muster anschließen. (X25-3120)	Die Stifte TEST kurzschließen und die Spannungsversorgung einschalten, um den Test-Modus zu aktivieren. Die Taste +10 drücken, dann öffnet sich der Träger, und die LD gibt Licht aus.	–	Stromwert + 5,5mA auf dem Lasertonabnehmer markiert. Wenn der Strom 40mA oder mehr über dem obigen Wert liegt, ist er defekt.	(b)
3	VCO	–	Einen Frequenzzähler an TP10(PLCK) anschließen. (X25-3120)	Die Spannungsversorgung aus-und dann wieder einschalten. Stop-Betriebsart	L13	4,32MHz (X25-3120)	(c)
4	FOKUS-FEHLERAUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1:RF Kanal 2:TE (X25-3120)	PLAY	FOKUS-FEHLERAUSGLEICH VR4 (X25-3120)	Optimales Augenmuster	(d)
5	TANGENTIAL	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1:RF Kanal 2:TE (X25-3120)	PLAY	Schraube an der rechten Seite des Mechanismus	Optimales Augenmuster	(d)
6	OPTISCHES GITTER (1)	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1:RF Kanal 2:TE (X25-3120)	Den Teststift kurzschließen und dabei die Spannungsversorgung einschalten, um den Testmodus zu aktivieren. Die CHECK-Taste drücken und prüfen, daß " 03oo " auf dem Display angezeigt wird.	Einstelloffnung unten am Laster-Tonabnehmer	Maximal-Amplitude (Siehe Photo 1 und 2.)	(d)
7	OPTISCHES GITTER (2) " Überprüfung der Polarität "	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1:RF Kanal 2:TE (X25-3120)	Die CLEAR-Taste drücken und den Spurhalte-Servo einschalten. Prüfen, daß " 04oo " auf dem Display angezeigt wird.	Einstellungsöffnung an der Unterseite des Laser-tonabnehmers	Überprüfen, daß das Augenmuster richtig ausgegeben wird.	(d)
8	OPTISCHES GITTER (3)	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF Kanal 2: SSPT (X25-3120)	Die PLAY-Taste drücken und prüfen, daß " 05oo " auf dem Display angezeigt wird.	Einstellungsöffnung an der Unterseite des Laser-tonabnehmers	Überprüfen, daß sie Photo 3 entsprechen. *Photo 4 zeigt das Beispiel eines defekten Tonabnehmers.	(e)
9	SPURHALTEFEHLER-AUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1:RF Kanal 2:TE (X25-3120)	Die CHECK-Taste drücken und prüfen, daß " 03oo " auf dem Display angezeigt wird.	TE BALANCE VR3 (X25-3120)	Symmetrie zwischen oberen und unteren Mustern oder Gleichstrom DC = 0±0,05V	(d)
10	FOKUSVERSTÄRKUNG	Testdisc Typ 4 Ein 900Hz, 50mVrms Signal an Stift 2 von CN4 an platine X25-3120 anlegen.	Eine Servo-Lehre verwenden ode ein 47kΩ, 470pF Tiefpaßfilter an Stift 1 von CN4 anschließen.	Die Spannungsversorgung aus-und dann wieder einschalten, dann die PLAY-Taste drücken.	FOKUSVERSTÄRKUNG VR5 (X25-3120)	50mVrms	(f)
11	SPURHALTE-VERSTÄRKUNG	Testdisc Typ 4 Ein 900Hz, 50mVrms Signal an Stift 4 von CN4 an platine X25-3120 anlegen.	Eine Servo-Lehre verwenden oder ein 47kΩ, 470pF Tiefpaßfilter an Stift 5 von CN4 anschließen.	PLAY	SPUHALTE-VERSTÄRKUNG VR6 (X25-3120)	50mVrms	(g)
12	DAC-AUSGANG	Testdisc Typ 4	Ein Wechselstrom-Voltmeter an die Ausgangsklemme(FIXED) anschließen.	Das 1kHz, 0dB Signal in Titel Nr.2 wiedergeben.	VR1: L VR2: R (X25-3120)	1,9~2,0Vrms	(h)

(Hinweis) Typ 4 Disc: SONY YEDS-18 Testdisc oder Äquivalent.

DP-880SG

ADJUSTMENT/REGLAGES/ABGLEICH

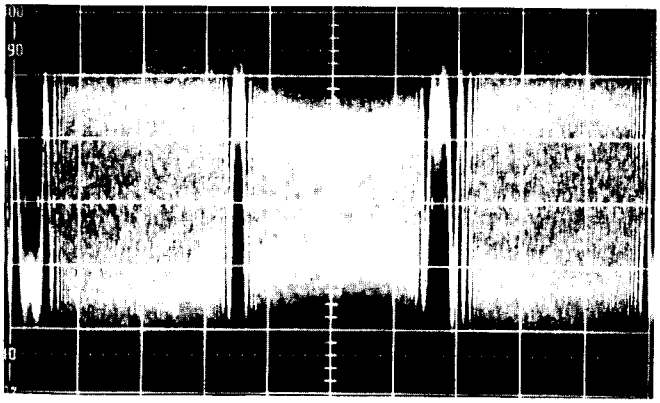
DIFFRACTION GRID ADJUSTMENT/REGLAGE DU RESEAU DE DIFFRACTION/BEUGUNGSGITTER-EINSTELLUNG



Correctly adjusted waveform
Forme d'onde correctement réglée
Richtig eingestellte Wellenform

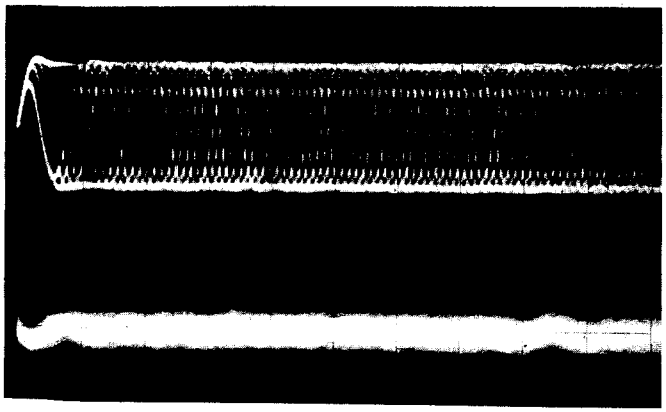
Photo 1
Photo 1
Foto 1

Tracking error waveform
Upper : 0.5V/div.
Lower : 20ms/div.
Forme d'onde d'erreur d'alignement
Supérieure : 0.5V/div.
Inférieure : 20ms/div.
Spurhaltefehler-Wellenform
Oben : 0.5V/Teilung
Unten : 20ms/Teilung



Incorrect (shifted) waveforms
Forme d'onde incorrecte (dérivée)
Falsche (verschobene) Wellenform

Photo 2
Photo 2
Foto 2

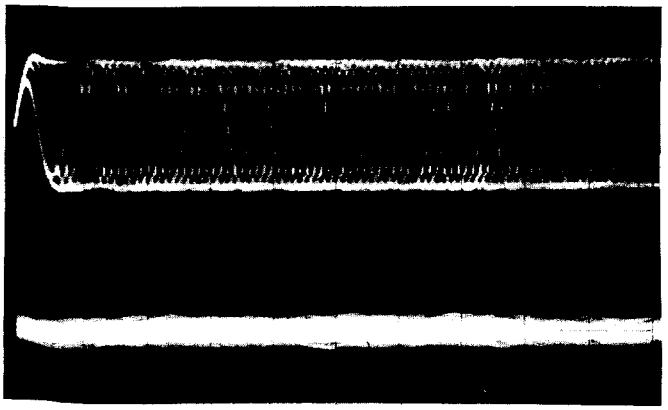


Correctly adjusted waveform
Forme d'onde correctement réglée
Richtig eingestellte Wellenform

Upper : RF signal 1V/div.
Lower : Sub spot beam signal 0.1V/div.
0.5μs/div.
Supérieure : signal HF 1V/div.
Inférieure : signal de rayon spot auxiliaire 0.1V/div.,
0.5μs/div.
Oben : HF-Signal 1V/Teilung
Unten : Nebenpunktstrahl-Signal 0,1V/Teilungs,
0,5μs/Teilung

Photo 3
Photo 3
Foto 3

17~18μs later
17~18μs us plus tard
17~18μs später



Waveform when the sub beam is shifted to the adjacent track.
Forme d'onde quand le rayon auxiliaire est décalé sur la piste adjacente.
Wellenform, wenn der Nebenstrahl zur benachbarten Spur verschoben ist.

Photo 4
Photo 4
Foto 4

VOLTAGE TABLES

X19-1140-01

Q101

8	5V

X25-3120-00

IC1

1	−0.7V
2	0V
3	0V
4	−9.5V
5	2.5V
6	2.5V
7	−0.2V
8	8.8V

IC2

1	2.1V
2	0V
3	0V
4	−11.8V
5	5V
6	5V
7	−2.2V
8	11.8V

IC3

1	5.5V
2	5V
3	5V
4	−11.7V
5	0V
6	0V
7	−6.2V
8	11.8V

IC4

1	5V
2	5V
3	5V
4	−11.7V
5	0V
6	0V
7	5.7V
8	5V

IC5

1	0.5V
2	0V
3	0V
4	−9.5V
5	4.7V
6	5V
7	−8.1V
8	8.8V

IC6

1	−0.5V
2	0V
3	0V
4	−11.8V
5	0V
6	0V
7	−0.5V
8	11.8V

IC7

1	−0.1V
2	0V
3	
4	−11.8V
5	0V
6	0V
7	0V
8	11.8V

IC8

1	−0.1V
2	0V
3	0V
4	−11.8V
5	0V
6	0V
7	0V
8	11.8V

IC9

1	−0.4V
2	2.5V
3	2.5V
4	−9.5V
5	0V
6	0V
7	0.6V
8	8.8V

IC10

1	−5.5V
2	0V
3	5V
4	–
5	0.2V
6	2.5V
7	2.0V
8	−5V
9	−0.1V
10	–
11	0V
12	0V
13	0V
14	–
15	1.9V
16	5.5V

IC11

1	−5.5V
2	0V
3	5V
4	–
5	0.2V
6	2.5V
7	2.0V
8	−5V
9	−0.1V
10	–
11	0V
12	0V
13	0V
14	–
15	1.9V
16	5.5V

IC12

1	0.2V	23	–
2	5V	24	–
3	–	25	–
4	0V	26	–
5	0.2V	27	
6	0V	28	0V
7	2.5V	29	0V
8	2.5V	30	–
9	–	31	0V
10	0V	32	0V
11	–	33	0V
12	1.5V	34	5V
13	1.0V	35	0V
14	0.9V	36	–
15	1.4V	37	5V
16	–	38	5V
17	5V	39	5V
18	–	40	2.5V
19	–	41	0V
20	0V	42	0V
21	–	43	0V
22	0V	44	0.3V

IC13

1	–	23	0V
2	–	24	0V
3	–	25	1.6V
4	–	26	1.6V
5	–	27	1.5V
6	5V	28	0V
7	5V	29	–
8	5V	30	–
9	5V	31	0V
10	0V	32	2.5V
11	4.9V	33	2.5V
12	0V	34	2V
13	2.4V	35	–
14	2.4V	36	–
15	2.9V	37	–
16	5V	38	–
17	5V	39	5V
18	0V	40	–
19	5V	41	–
20	0V	42	–
21	5V	43	–
22	0V	44	–

IC14

1	0V	21	–	41	2.4V	61	–
2	0V	22	–	42	2.4V	62	–
3	0V	23	0V	43	2.4V	63	–
4	0.1V	24	0V	44	2.4V	64	–
5	4.2V	25	2.5V	45	2.7V	65	–
6	4.5V	26	0V	46	2.3V	66	–
7	–	27	2.1V	47	2.4V	67	5V
8	0V	28	0V	48	2.8V	68	–
9	2.5V	29	0.6V	49	4.3V	69	–
10	0V	30	0.6V	50	2V	70	1.6V
11	2.5V	31	0.6V	51	1.5V	71	–
12	0V	32	0.6V	52	0V	72	–
13	5V	33	5V	53	1.8V	73	5V
14	5V	34	2.7V	54	2.3V	74	–
15	5V	25	2.7V	55	0V	75	–
16	4.9V	36	2.2V	56	0V	76	2.9V
17	4.5V	37	4.3V	57	5V	77	–
18	0V	38	2.4V	58	0V	78	2.4V
19	5V	39	2.4V	59	0V	79	–
20	0V	40	2.4V	60	–	80	2.4V

IC15

1	2.4V
2	2.4V
3	2.4V
4	2.4V
5	2.4V
6	2.4V
7	2.4V
8	2.7V
9	2.7V
10	0.6V
11	0.6V
12	0V
13	0.6V
14	0.6V
15	2.7V
16	2.2V
17	4.3V
18	2V
19	2.3V
20	2V
21	4.3V
22	2.8V
23	2.4V
24	5V

IC16

1	−16.2V	33	–
2	−9.2V	34	–
3	−11.5V	35	0V
4	−16.2V	38	0V
5	0V	37	0V
6	2.5V	38	0V
7	0V	39	4.9V
8	0V	40	−30V
9	4.9V	41	−30V
10	0V	42	−30V
11	0V	43	−30V
12	0V	44	0.6V
13	0V	45	−30V
14	5V	46	−30V
15	5V	47	−30V
16	5V	48	−30V
17	–	49	−30V
18	0.6V	50	−30V
19	5V	51	−30V
20	0.6V	52	−30V
21	0V	53	0.6V
22	0V	54	−19.6V
23	0V	55	−17V
24	0V	56	−32.4V
25	5V	57	−5V
26	5V	58	−22.2V
27	5V	59	−17.4V
28	0V	60	−12.5V
29	–	61	−32.2V
30	1.5V	62	−19.4V
31	–	63	−14V
32	0V	64	5V

IC17

1	0V
2	0V
3	0V
4	–
5	–
6	0V
7	0V
8	0V
9	0V
10	0V
11	0V
12	0V
13	0V
14	–
15	−1.1V
16	1.2V
17	−5V
18	0V
19	0V
20	0V
21	4.9V
22	4.4V
23	−2.8V
24	0V
25	0V
26	0.8V
27	4.2V
28	0.2V
29	–
30	5V

IC18

1	0V
2	0V
3	0V
4	0V
5	−4.5V
6	0V
7	−5V
8	0V
9	5V
10	0V
11	0V
12	0V
13	0V
14	0V
15	0V
16	5V

IC19

1	0V
2	0V
3	0V
4	0V
5	0V
6	4.5V
7	4.9V
8	5V
9	5V
10	5V
11	4.4V
12	0V
13	0V
14	−4.4V
15	5V
16	0V
17	−5V
18	5V
19	0V
20	0V
21	0V
22	0V
23	0V
24	0V
25	0V
26	5V
27	−0.3V
28	0V
29	0V
30	0V

IC20

1	0V
2	0V
3	−9.5V
4	0.1V
5	8.7V

IC22

1	5V
2	2.2V
3	2.2V
4	2.2V
5	5V
6	2.2V
7	0V
8	2.2V
9	5V
10	2.2V
11	2.2V
12	4.9V
13	2.1V
14	5V

IC23

1	−0.4V
2	0V
3	0V
4	−9.5V
5	0V
6	0V
7	0.6V
8	8.8V

Q1

E	8.8V
C	5V
B	8.1V

Q2

E	−9.5V
C	−5V
B	−8.9V

Q3

E	11.8V
C	18.1V
B	12.4V

VOLTAGE TABLES

Q4

E	-11.8V
C	-17.8V
B	-12.4V

Q5

E	0V
C	4.9V
B	-6.4V

Q6

E	0V
C	8.8V
B	0.5V

Q7

E	0V
C	-9.5V
B	0.5V

Q8

E	-24.5V
C	-40.5V
B	-22.9V

Q9

E	-5.1V
C	-22.9V
B	-5.7V

Q10

E	5V
C	-11.7V
B	5V

Q11

E	-11.7V
C	5.4V
B	-11.7V

Q12

E	-11.8V
C	0V
B	-11.7V

Q13

E	0V
C	0V
B	0.7V

Q14

E	0V
C	0V
B	0.7V

Q15

E	-0.1V
C	-17.8V
B	—

Q16

E	0.1V
C	-17.8V
B	—

Q17

E	0.1V
C	18.1V
B	—

Q18

E	0.1V
C	18.1V
B	—

Q19

E	0V
C	8.8V
B	0.6V

Q20

E	0V
C	-9.5V
B	-0.6V

Q21

E	5V
C	-27.1V
B	4.9V

Q22

E	0V
C	4.3V
B	0.6V

Q23

E	5V
C	5V
B	5.7V

Q24

E	-5.5V
C	-11.7V
B	-6.2V

Q25

1	8.8V
2	0.6V
3	0.5V
4	-0.4V
5	-9.5V
6	0V
7	0V
8	0V

X25-3130-00

IC1

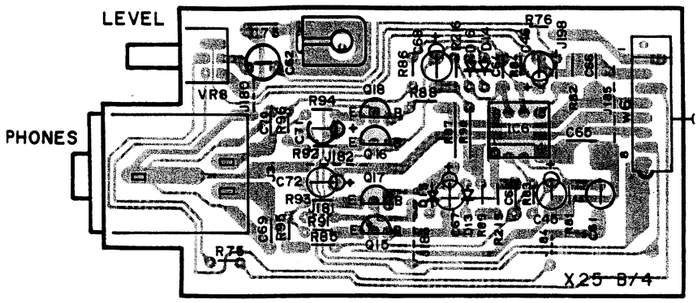
1	3.1V
2	3.1V
3	3.1V
4	3.1V
5	0V
6	3.1V
7	2.2V
8	0.5V
9	5V

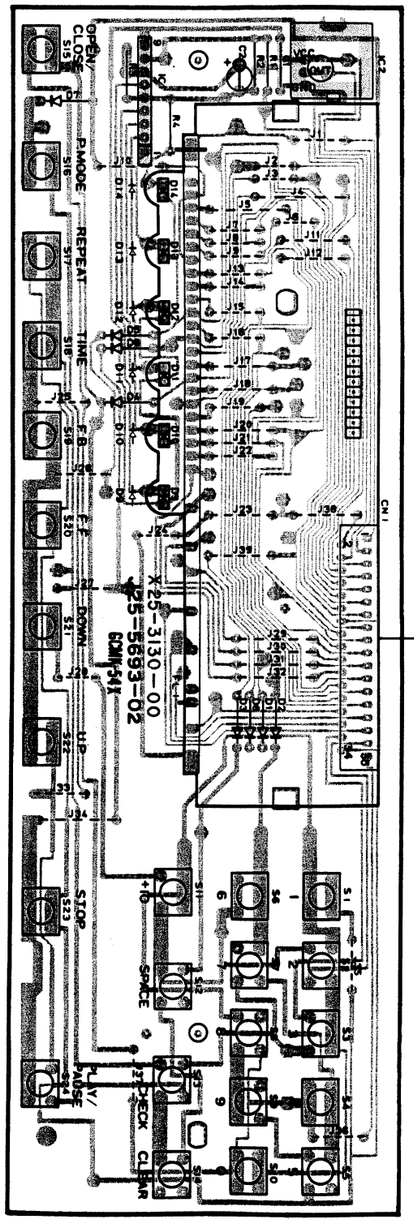
IC2

G	0V
OUT	4.9V
Vcc	5V

PC BOARD (Component side view)

ELECTRIC SECTION UNIT (X25-3120-11) (B/4)





CONTROL SECTION UNIT (X25-3130-00)

(b) Laser pickup operating current
: +5.5 mA current value labeld on the laser pickup

DC ammeter

(C) VCO: 4.32 MHz

Frequency counter

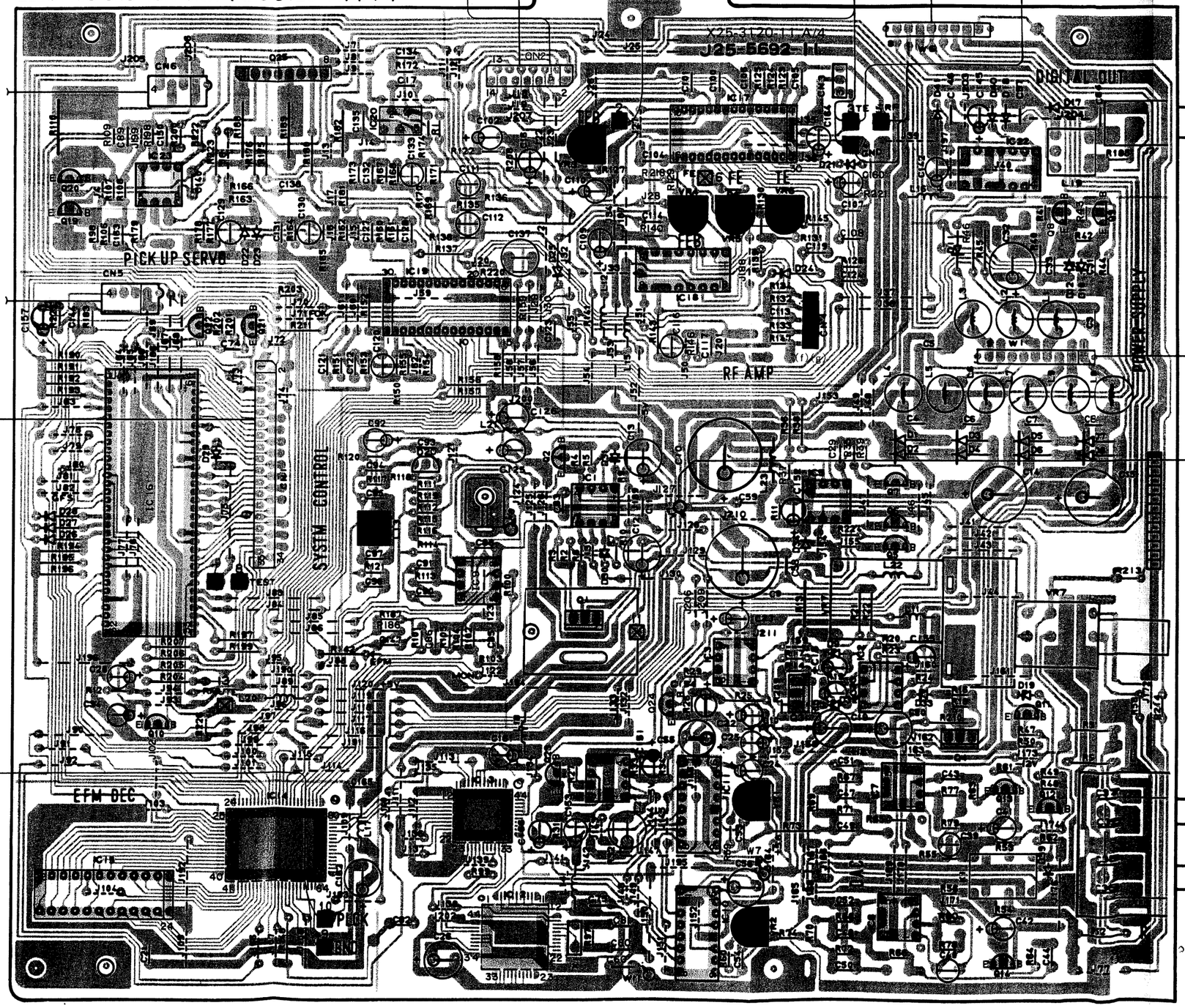
(d) Focus error balance
:Optimum eye pattern
Tangential
: Optimum eye pattern
Diffraction grating (1)
: Maximum amplitude (See photo 1 and 2)

(e) Diffraction grating (3)
: Check that they are as photo 3

Oscilloscope

Oscilloscope

ELECTRIC SECTION UNIT (X25-3120-11) (A/4)



FRONT

(d) Focus error balance
:Optimum eye pattern
Tangential
: Optimum eye pattern
Diffraction grating (1)
: Maximum amplitude (See photo 1 and 2)

(e) Diffraction grating (3)
: Check that they are as photo 3

Diffraction grating (2)
: Confirm that the eye pattern is presented correctly
Tracking error balance
: Symmetry between upper and lower patterns, or DC ±0.05 V

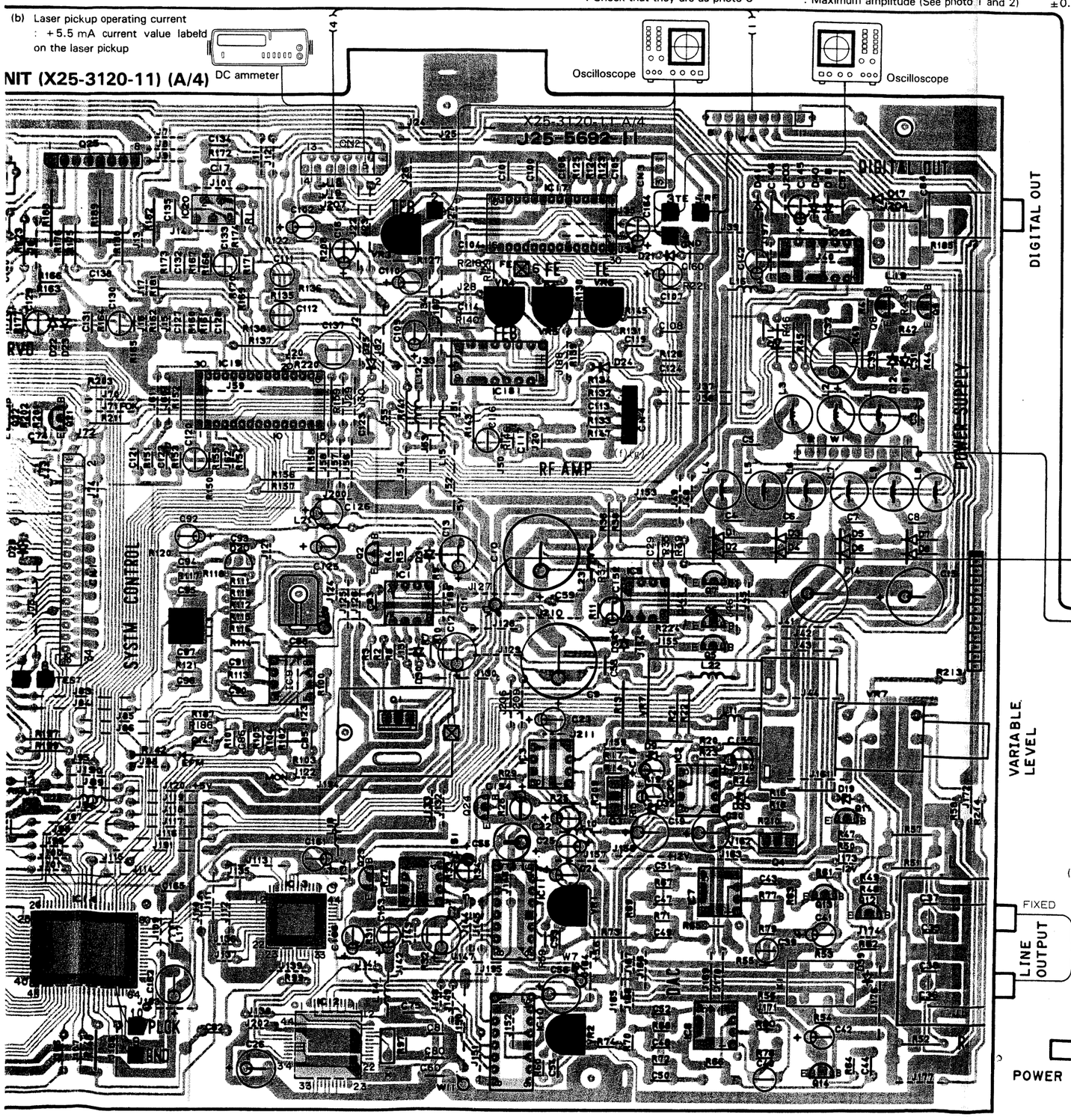
(b) Laser pickup operating current
: +5.5 mA current value labeld on the laser pickup

DC ammeter

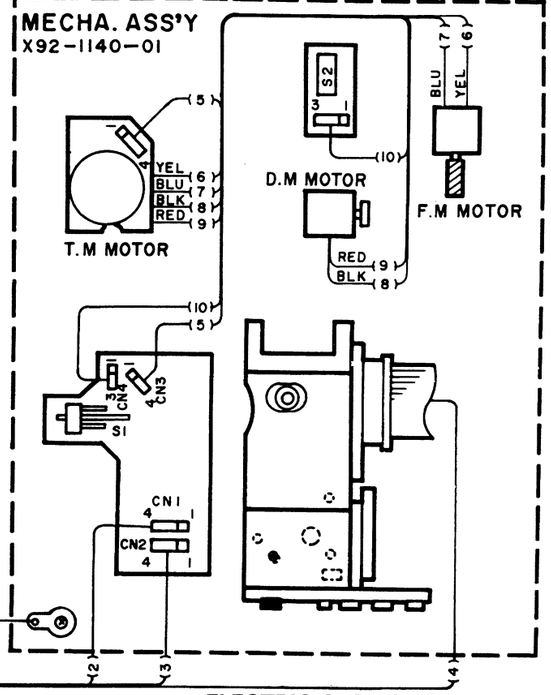
Oscilloscope

Oscilloscope

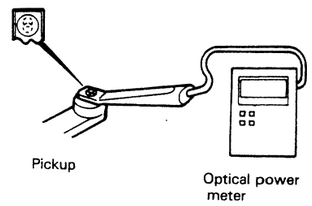
NIT (X25-3120-11) (A/4)



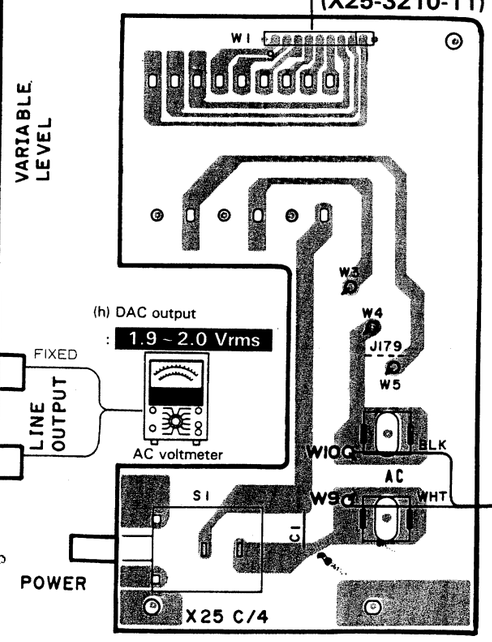
MECHANISM ASS'Y (X92-1140-01)



(a) Laser power: 0.1 mW

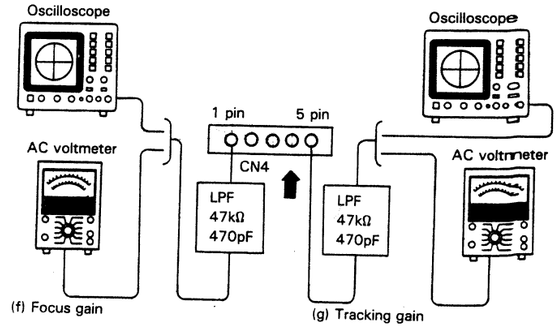


ELECTRIC SECTION UNIT (X25-3210-11) (C/4)



(f) Focus gain: 50 mVrms

(g) Tracking gain: 50 mVrms



Refer to the schematic diagram for the values of resistors and capacitors.

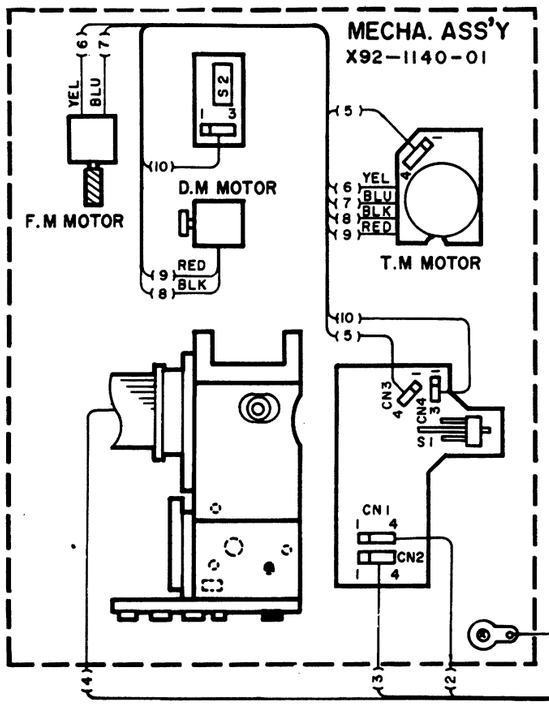
PC BOARD (Foil side view)

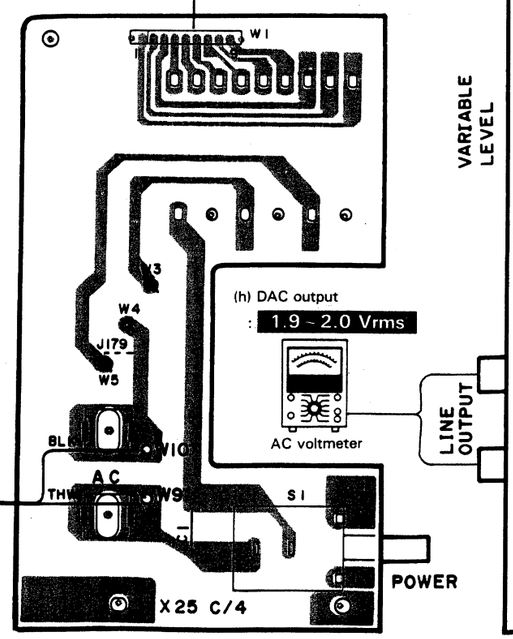
(d) Focus error balance
:Optimum eye pattern
Tangential
: Optimum eye pattern
Diffraction grating (1)
: Maximum amplitude (See photo 1 and 2)

Diffraction grating (2)
: Confirm that the eye pattern is presented correctly
Tracking error balance
: Symmetry between upper and lower patterns, or DC ±0.05 V

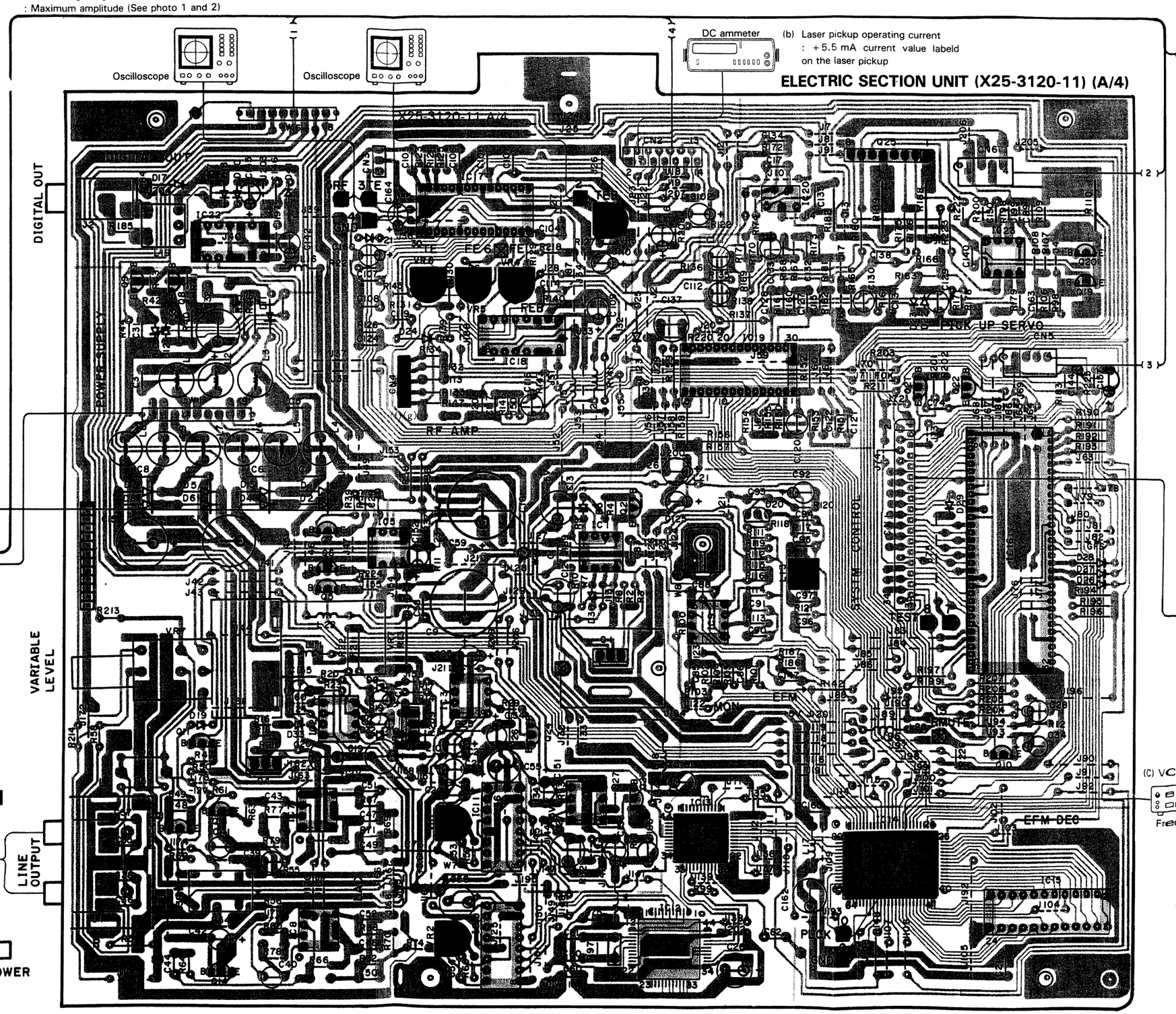
(e) Diffraction grating (3)
: Check that they are as photo 3

MECHANISM ASS'Y (X92-1140-01)





ELECTRIC SECTION UNIT (X25-3210-11) (C/4)



pattern is presented correctly

upper and lower patterns, or DC

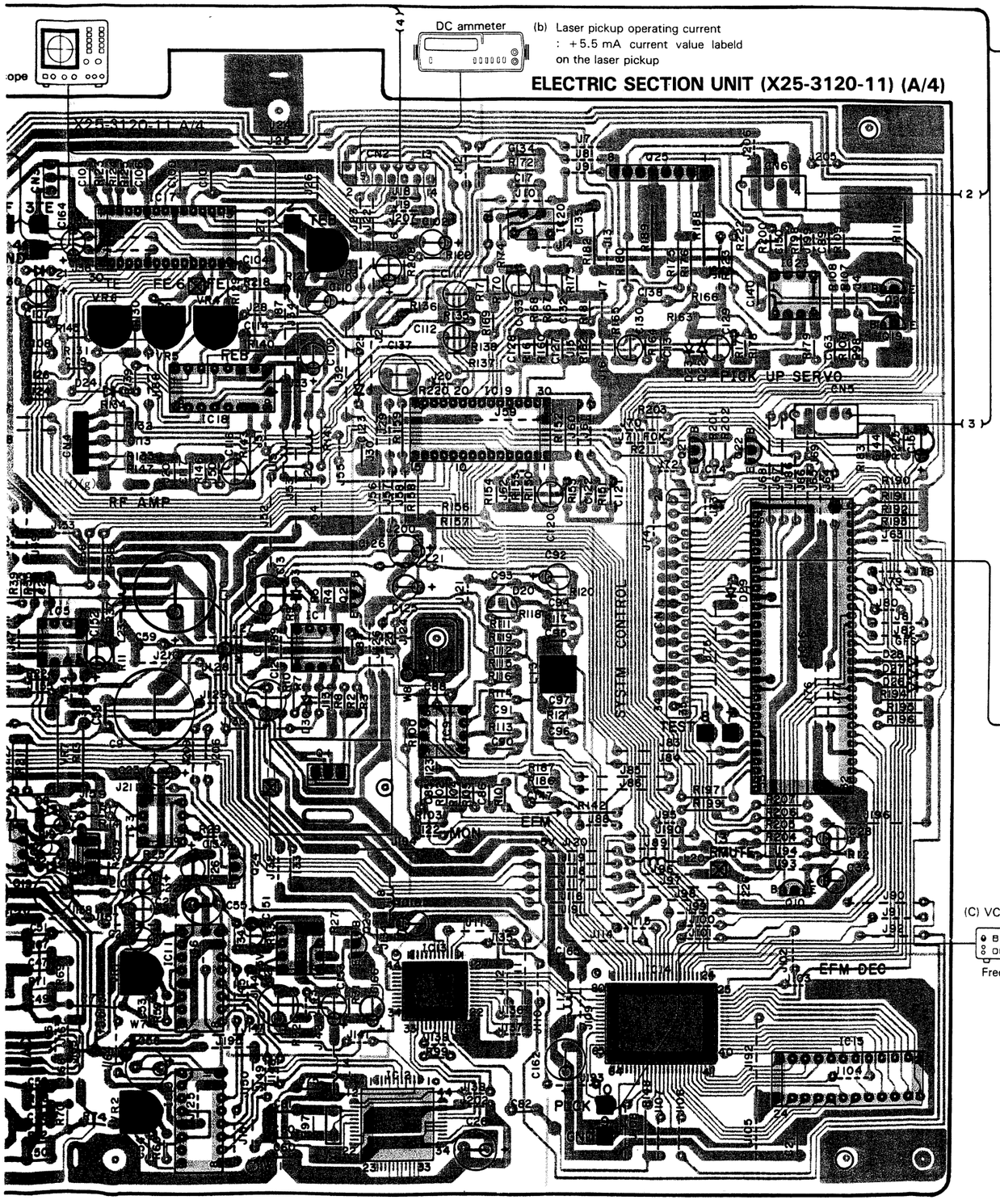
(e) Diffraction grating (3)
: Check that they are as photo 3

ope

DC ammeter

(b) Laser pickup operating current
: +5.5 mA current value labeld on the laser pickup

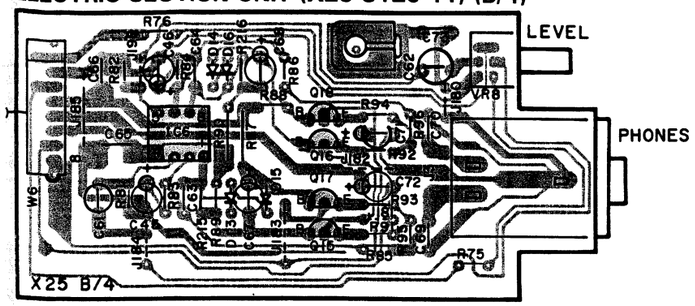
ELECTRIC SECTION UNIT (X25-3120-11) (A/4)

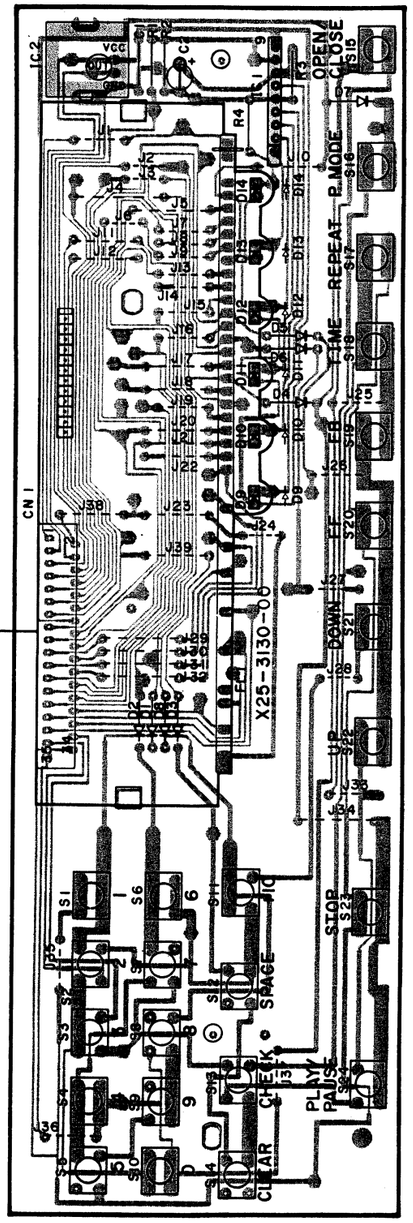


(C) VCO: 4.32 MHz

Frequency counter

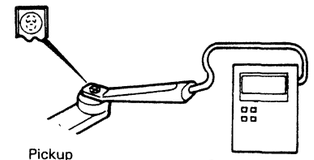
ELECTRIC SECTION UNIT (X25-3120-11) (B/4)





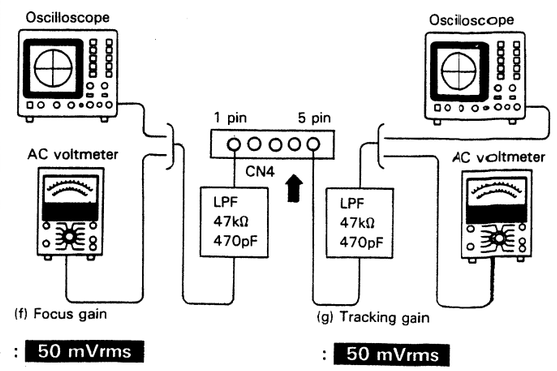
FRONT

(a) Laser power: 0.1 mW



(f) Focus gain: 50 mVrms

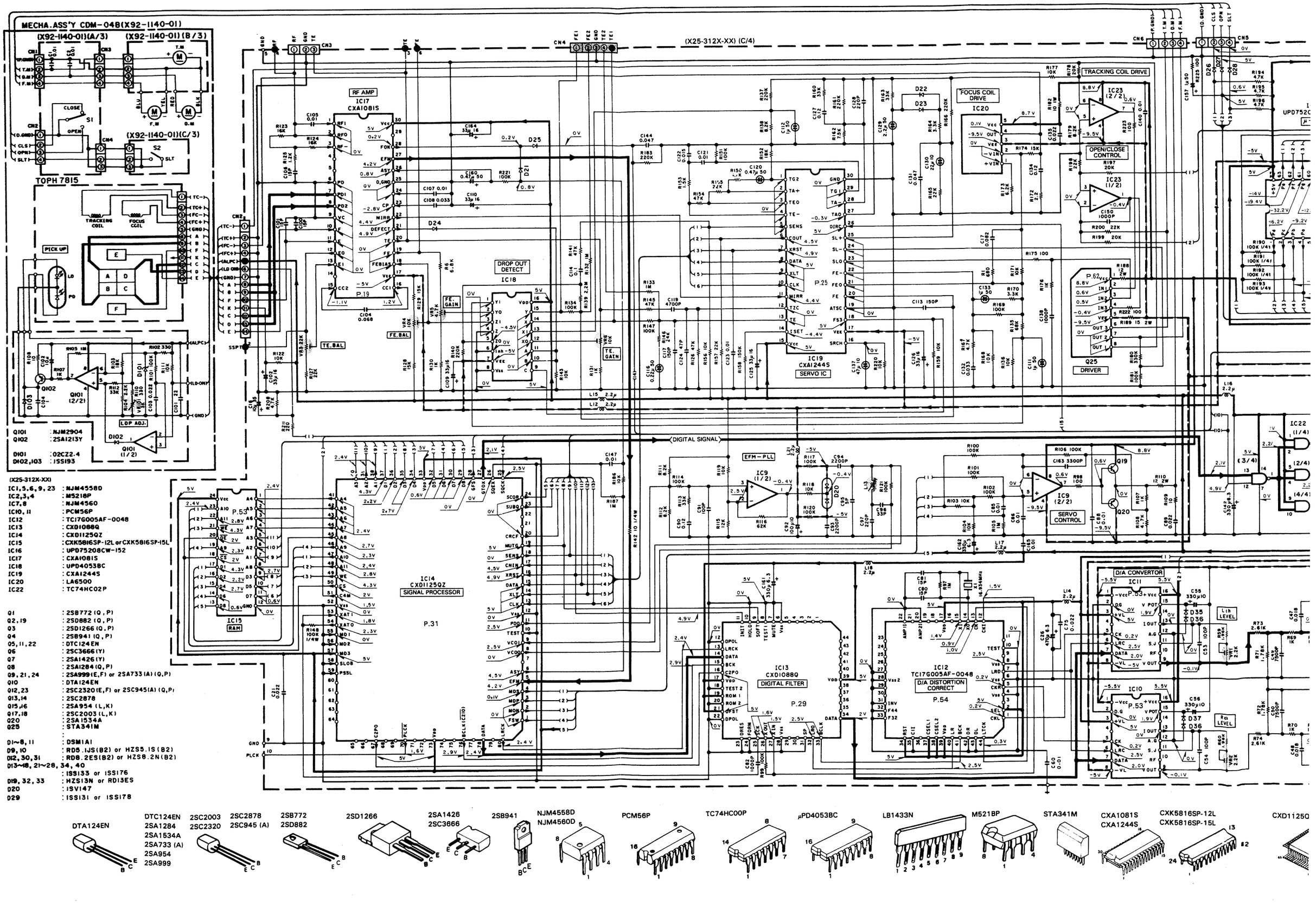
(g) Tracking gain: 50 mVrms



DP-880SG (K)

Refer to the schematic diagram for the values of resistors and capacitors.

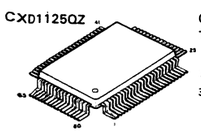
CONTROL SECTION UNIT (X25-3130-00)


MECHA.ASS'Y CDM-048(X92-1140-01)
(X92-1140-01)(A/3)
(X92-1140-01)(B/3)
(X92-1140-01)(C/3)
TOPH 7815
(X25-312X-XX) (C/4)
RF AMP
IC17 CXA1081S
DROP OUT DETECT
IC18
IC19 CXA1244S
SERVO IC
FOCUS COIL DRIVE
IC20
TRACKING COIL DRIVE
IC23 (2/2)
OPEN/CLOSE CONTROL
IC23 (1/2)
Q25
DRIVER
IC14 CXD1125QZ
SIGNAL PROCESSOR
P.31
IC15
RAM
P.53
IC13 CXD1088Q
DIGITAL FILTER
P.29
IC12 TC17G005AF-0048
D/A DISTORTION CORRECT
P.54
IC11
IC10
D/A CONVERTOR
EFM-PLL
IC9 (1/2)
IC9 (2/2)
SERVO CONTROL
Q19
Q20
DIGITAL SIGNAL
Lch LEVEL
Rch LEVEL
DIO1
DIO2
Q101 (1/2)
LDP ADJ.
Q101 : NJM2904
Q102 : 2SA1213Y
DI01 : 02CZ2.4
DI02,103 : 1SS193
(X25-312X-XX)
IC1,5,6,9,23 : NJM4558D
IC2,3,4 : M5218P
IC7,8 : NJM4560
IC10,11 : PCM56P
IC12 : TC17G005AF-0048
IC13 : CXD1088Q
IC14 : CXD1125QZ
IC15 : CXK5816SP-12L or CXK5816SP-15L
IC16 : UPD75208CW-152
IC17 : CXA1081S
IC18 : UPD40538C
IC19 : CXA1244S
IC20 : LA6500
IC22 : TC74HC02P
Q1 : 2SB772(Q,P)
Q2,19 : 2SD882(Q,P)
Q3 : 2SD1266(Q,P)
Q4 : 2SB941(Q,P)
Q5,11,22 : DTC124EN
Q6 : 2SC3666(Y)
Q7 : 2SA1426(Y)
Q8 : 2SA1284(Q,P)
Q9,21,24 : 2SA999(E,F) or 2SA733(A)(Q,P)
Q10 : DTA124EN
Q12,23 : 2SC2320(E,F) or 2SC945(A)(Q,P)
Q13,14 : 2SC2878
Q15,16 : 2SA954(L,K)
Q17,18 : 2SC2003(L,K)
Q20 : 2SA1534A
Q25 : STA341M
DI~8,11 : DSM1A1
DI9,10 : RD5.1JS(B2) or HZS5.1S(B2)
DI2,30,31 : RD8.2ES(B2) or HZS8.2N(B2)
DI3~18,21~28,34,40 : 1SS133 or 1SS176
DI9,32,33 : HZS13N or RD13ES
D20 : 1SV147
D29 : 1SS131 or 1SS178
DTA124EN
DTC124EN
2SA1284
2SA1534A
2SA733 (A)
2SA954
2SA999
2SC2003
2SC2320
2SC2878
2SC945 (A)
2SB772
2SD882
2SD1266
2SA1426
2SC3666
2SB941
NJM4558D
NJM4560D
PCM56P
TC74HC00P
μPD4053BC
LB1433N
M521BP
STA341M
CXA1081S
CXA1244S
CXK5816SP-12L
CXK5816SP-15L
CXD1125Q

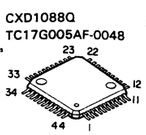
J K L M N O P Q R S

Note: The page numbers in the IC corresponds to the page numbers of the circuit description.

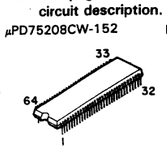
CXD1125QZ



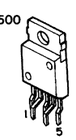
CXD1088Q
TC17G005AF-0048



μPD75208CW-152



LA6500



DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

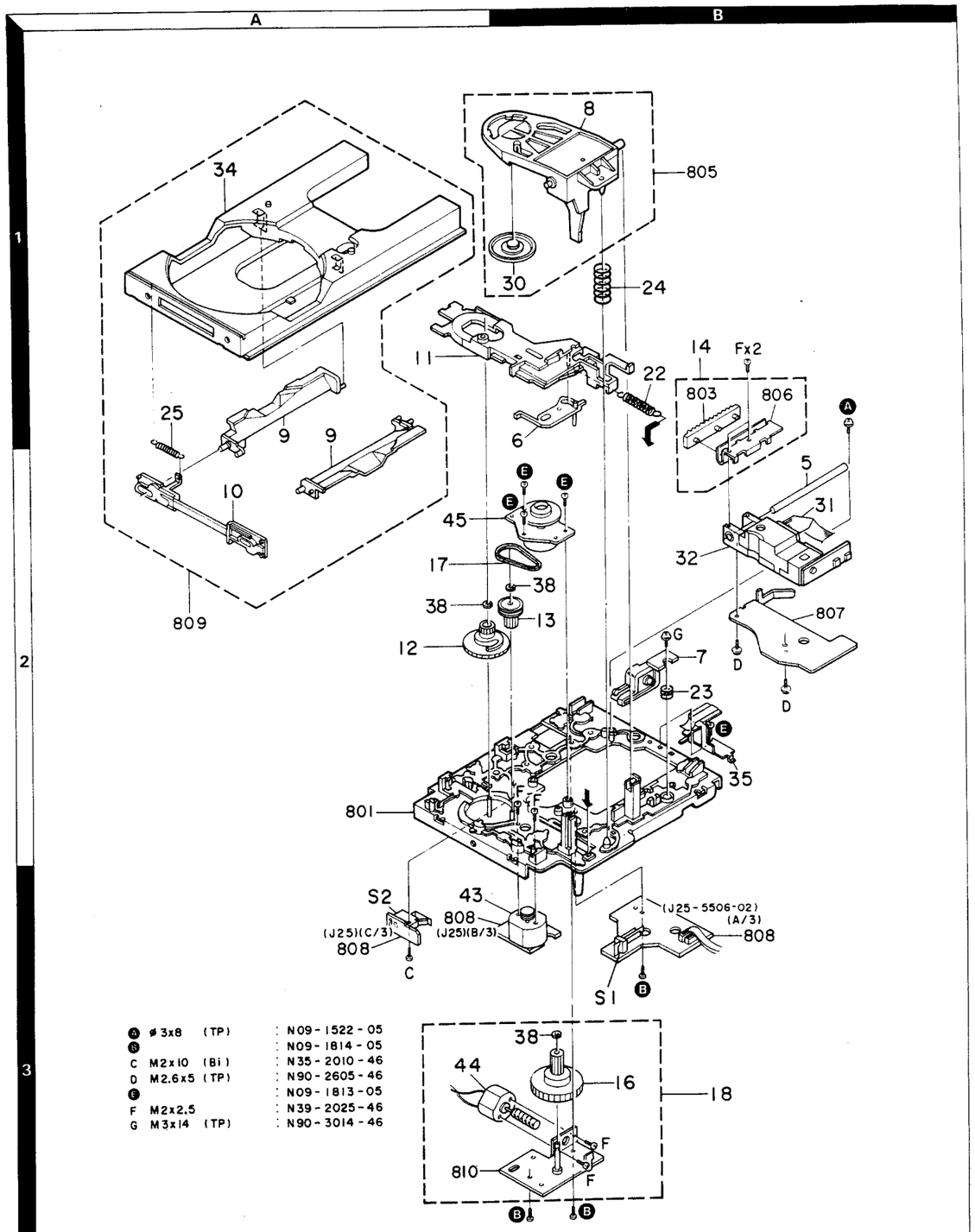
DP-880SG (K)

DP-880SG

KENWOOD

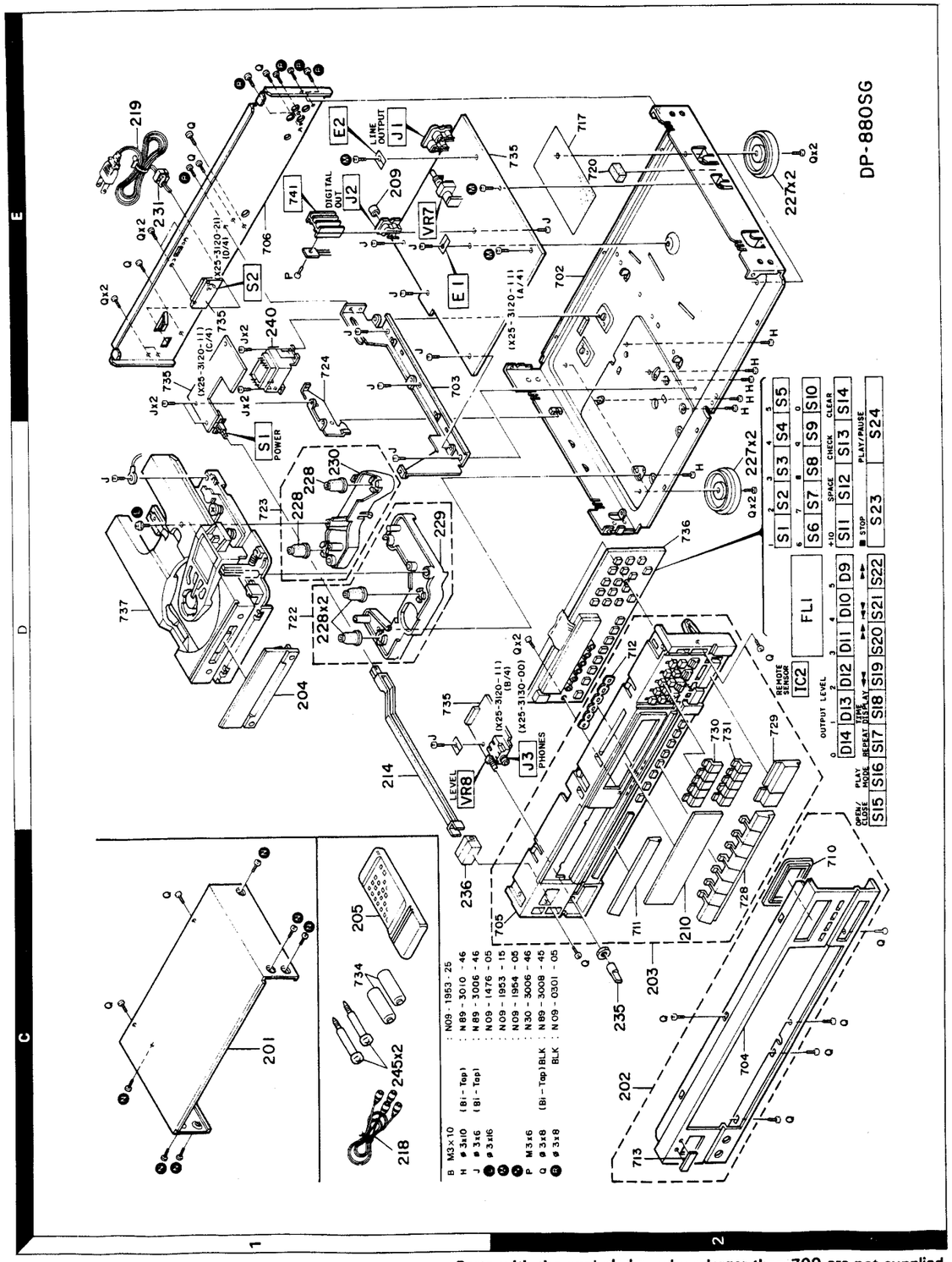
DP-880SG DP-880SG

EXPLODED VIEW (MECHANISM)



Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

	Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
				DP-880SG (Japan made)			
	201	1C		A01-1514-02	METALLIC CABINET		
	202	2C	*	A20-5347-02	PANEL ASSY		
	203	2C	*	A22-0916-02	SUB PANEL ASSY		
	204	1D	*	A29-0115-03	PANEL (TRAY)		
	205	1C	*	A70-0181-05	REMOTE CONTROLLER ASSY		
	209	1E		B09-0068-05	CAP (DIGITAL OUT)		
	210	2C	*	B10-0899-04	FRONT GLASS (DISPLAY)		
	-			B46-0092-03	WARRANTY CARD	K	
	-			B46-0094-03	WARRANTY CARD	UUE	
	-			B46-0095-03	WARRANTY CARD	UUE	
	-			B46-0096-13	WARRANTY CARD	X	
	-			B46-0121-03	WARRANTY CARD	P	
	-			B46-0122-13	WARRANTY CARD	E	
	-			B46-0143-03	WARRANTY CARD	T	
	-		*	B50-8534-00	INSTRUCTION MANUAL(ENGLISH)		
	-		*	B50-8535-00	INSTRUCTION MANUAL(FRENCH)	PMXE	
	-		*	B50-8536-00	INSTRUCTION MANUAL(SPANISH)	M	
	-		*	B50-8537-00	INSTRUCTION MANUAL(G.D.I)	E	
	-			B58-0223-04	CAUTION CARD (PRE-SET 120V)	U	
	-			B58-0269-04	CAUTION CARD	K	
	-			B58-0400-04	CAUTION CARD		
	-			B58-0513-04	CAUTION CARD (PRESET220-240)	UE	
	-			B58-0849-04	CAUTION CARD		
	-			B59-0092-00	SERVICE DIRECTORY	UUE	
	214	1D		D21-1148-03	EXTENSION SHAFT		
	218	1C		E30-0505-05	AUDIO CORD		
△	219	1E		E30-2275-05	AC POWER CORD	X	
△	219	1E		E30-2276-05	AC POWER CORD	T	
△	219	1E		E30-2277-05	AC POWER CORD	E	
△	219	1E	*	E30-2284-05	AC POWER CORD	UMUE	
△	219	1E	*	F30-2405-05	AC POWER CORD	KP	
	-		*	H01-7662-04	ITEM CARTON CASE		
	-		*	H10-3383-12	POLYSTYRENE FOAMED FIXTURE		
	-		*	H10-3384-12	POLYSTYRENE FOAMED FIXTURE		
	-			H10-3512-04	POLYSTYRENE FOAMED FIXTURE		
	-			H20-0417-14	PROTECTION COVER(460X370X360)	M	
	-			H25-0224-04	PROTECTION BAG (800X400X0.03)	KPUUEX	
	-			H25-0224-04	PROTECTION BAG (800X400X0.03)	TE	
	-			H25-0232-04	PROTECTION BAG (235X350X0.03)		
	227	2D,2E		J02-0188-15	INSULATOR (FOOT)		
	228	1D		J02-0191-05	INSULATOR (HOLDER)		
	229	1D	*	J19-2687-03	HOLDER (FRONT)		
	230	1D	*	J19-2688-23	HOLDER (REAR)		
△	231	1E		J42-0083-05	POWER CORD BUSHING		
	235	2C		K29-2201-04	KNOB (LEVEL)		
	236	1C		K29-2725-04	KNOB (BUTTON) POWER		
△	240	1E	*	L01-4751-05	POWER TRANSFORMER	KP	
△	240	1E	*	L01-4752-05	POWER TRANSFORMER	E	
△	240	1E	*	L01-4754-05	POWER TRANSFORMER	UMUE	
△	240	1E	*	L01-4757-05	POWER TRANSFORMER	XT	

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	245	1C		N09-1680-05	STEPPED SCREW		
	L	1F		N09-1476-05	MACHINE SCREW (Ø3X16)		
	M	1C	*	N09-1953-25	MACHINE SCREW (M3X10)		
	N	1C	*	N09-1954-05	MACHINE SCREW (CASE)		
	R	1E		N09-0301-05	TAPTITE SCREW (Ø3X8)		
				DP-880SG (Singapore made)			
	201	1C		A01-1514-02	METALLIC CABINET		
	202	2C	*	A20-5347-02	PANEL ASSY		
	203	2C	*	A22-0916-02	SUB PANEL ASSY		
	204	1D	*	A29-0115-03	PANEL (TRAY)		
	205	1C	*	A70-0181-05	REMOTE CONTROLLER ASSY		
	209	1E		B09-0068-05	CAP (DIGITAL OUT)		
	210	2C	*	B10-0899-04	FRONT GLASS (DISPLAY)		
	-			B46-0122-13	WARRANTY CARD	E	
	-			B46-0143-03	WARRANTY CARD	T	
	-		*	B50-8756-00	INSTRUCTION MANUAL(ENGLISH)		
	-		*	B50-8757-00	INSTRUCTION MANUAL(FRENCH)	E	
	-		*	B50-8758-00	INSTRUCTION MANUAL(G.D.I)	E	
	-			B58-0400-04	CAUTION CARD		
	-			B58-0849-04	CAUTION CARD		
	214	1D		D21-1148-03	EXTENSION SHAFT		
	218	1C		E30-0505-05	AUDIO CORD		
△	219	1E		E30-2276-05	AC POWER CORD	T	
△	219	1E		E30-2277-05	AC POWER CORD	E	
	-		*	H01-7775-04	ITEM CARTON CASE		
	-		*	H10-3562-02	POLYSTYRENE FOAMED FIXTURE		
	-		*	H10-3563-02	POLYSTYRENE FOAMED FIXTURE		
	-			H10-3564-04	POLYSTYRENE FOAMED FIXTURE		
	-			H25-0224-04	PROTECTION BAG (800X400X0.03)		
	-			H25-0232-04	PROTECTION BAG (235X350X0.03)		
	227	2D,2E		J02-0188-15	INSULATOR (FOOT)		
	228	1D		J02-0191-05	INSULATOR (HOLDER)		
	229	1D	*	J19-2687-03	HOLDER (FRONT)		
	230	1D	*	J19-2688-23	HOLDER (REAR)		
△	231	1E		J42-0083-05	POWER CORD BUSHING		
	235	2C		K29-2201-04	KNOB (LEVEL)		
	236	1C		K29-2725-04	KNOB (BUTTON) POWER		
△	240	1E	*	L01-4752-05	POWER TRANSFORMER	E	
△	240	1E	*	L01-4757-05	POWER TRANSFORMER	T	
	245	1C		N09-1680-05	STEPPED SCREW		
	L	1D		N09-1476-05	MACHINE SCREW (Ø3X16)		
	M	1C		N09-1953-25	MACHINE SCREW (M3X10)		
	N	1C		N09-1954-05	MACHINE SCREW (CASE)		
	R	1E		N09-0301-05	TAPTITE SCREW (Ø3X8)		
	251	1C		W09-0022-05	BATTERY		
	ELECTRIC UNIT (X25-312X-XX) 0-11: K,P,X,T 0-21: U,M,UE 2-71: E 0-21: S(T) 2-72: S(E)						
△	C1			C91-0647-05	CERAMIC 0.01UF P		
	C3 -8			CK45FF1H103Z	CERAMIC 0.01UF Z		
	C9 ,10			CE04KW1C332M	ELECTRO 3300UF 16WV		
	C11			CK45FF1H103Z	CERAMIC 0.01UF Z		
	C12 ,13			CE04KW0J471M	ELECTRO 470UF 6.3WV		

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C14 ,15			CE04KW1E102M	ELECTRO 1000UF 25WV		
C16			CE04KW1V100M	ELECTRO 10UF 35WV		
C17			CF92FV1H823J	MF 0.082UF J		
C18			CE04KW1V100M	ELECTRO 10UF 35WV		
C19 ,20			CE04KW1C331M	ELECTRO 330UF 16WV		
C21			CK45FF1H223Z	CERAMIC 0.022UF Z		
C22 ,23			CE04KW1C470M	ELECTRO 47UF 16WV		
C24			CE04KW1A101M	ELECTRO 100UF 10WV		
C25			CE04KW1A101M	ELECTRO 100UF 10WV		
C26 ,27			CE04KW0J471M	ELECTRO 470UF 6.3WV		
C28			CE04KW1V4R7M	ELECTRO 4.7UF 35WV		
C29			CK45FF1H103Z	CERAMIC 0.010UF Z		
C30			CE04KW1C220M	ELECTRO 22UF 16WV		
C31			CK45FF1H103Z	CERAMIC 0.010UF Z		
C32			CE04KW1J101M	ELECTRO 100UF 63WV		
C33			CK45FF1H103Z	CERAMIC 0.010UF Z		
C34		*	CE04KW1A331M	ELECTRO 330UF 10WV		
C35 -38			CK45FB1H102K	CERAMIC 1000PF K		
C39 ,40			C90-1334-05	NP-ELEC 47UF 10WV		
C41 ,42			CE04KW1V100M	ELECTRO 10UF 35WV		
C43 ,44			CQ93HP2A183J	MYLAR 0.018UF J		
C45 ,46			CE04KW1A470M	ELECTRO 47UF 10WV		
C47 ,48			CQ93HP2A183J	MYLAR 0.018UF J		
C49 ,50			CQ93HP2A752J	MYLAR 7500PF J		
C51 ,52			CQ93HP2A102J	MYLAR 1000PF J		
C53			CQ09FS1H101J	POLYSTY 100PF J		
C54			CQ09FS1H101J	POLYSTY 100PF J		
C55		*	CE04KW1A331M	ELECTRO 330UF 10WV		
C56			CE04KW1A331M	ELECTRO 330UF 10WV		
C57			CK45FF1H472Z	CERAMIC 4700PF Z		
C58 ,59			CK45FF1H223Z	CERAMIC 0.022UF Z		
C60			CK45FF1H103Z	CERAMIC 0.010UF Z		
C61 ,62			C90-1351-05	NP-ELEC 3.3UF 50WV		
C63 ,64			CC45FSL1H220J	CERAMIC 22PF J		
C65 ,66			CF92FV1H103J	MF 0.010UF J		
C67 ,68			CE04KW1A101M	ELECTRO 100UF 10WV		
C69 ,70			CF92FV1H102J	MF 1000PF J		
C71 ,72			CE04KW1V4R7M	ELECTRO 4.7UF 35WV		
C73 ,74			CK45FF1H103Z	CERAMIC 0.010UF Z		
C75			CK45FF1H223Z	CERAMIC 0.022UF Z		
C80 ,81		*	C91-0980-05	CERAMIC 15PF G		
C82			CK45FB1H102K	CERAMIC 1000PF K		
C83			CK45FF1H103Z	CERAMIC 0.010UF Z		
C84			CC45FSL1H101J	CERAMIC 100PF J		
C85 ,86			CF92FV1H103J	MF 0.010UF J		
C88			CK45FF1H103Z	CERAMIC 0.010UF Z		
C89			CF92FV1H223J	MF 0.022UF J		
C90			CF92FV1H124J	MF 0.12UF J		
C91			CC45FSL1H101J	CERAMIC 100PF J		
C92			CE04KW1A101M	ELECTRO 100UF 10WV		
C93 ,94			CK45FB1H222K	CERAMIC 2200PF K		
C95			CC45FUJ1H050C	CERAMIC 5.0PF C		
C96			CC45FUJ1H330J	CERAMIC 33PF J		
C97			CC45FUJ1H221J	CERAMIC 220PF J		
C100,101			CC45FSL1H150J	CERAMIC 15PF J		

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C102			CE04KW1C330M	ELECTRO 33UF 16WV		
C104			CF92FV1H683J	MF 0.068UF J		
C105			CK45FF1H103Z	CERAMIC 0.010UF Z		
C106			CC45FSL1H150J	CERAMIC 15PF J		
C107			CF92FV1H103J	MF 0.010UF J		
C108			CF92FV1H333J	MF 0.033UF J		
C109,110			CE04KW1C330M	ELECTRO 33UF 16WV		
C111,112			C90-1349-05	NP-ELEC 1UF 50WV		
C113			CC45FSL1H151J	CERAMIC 150PF J		
C114			CF92FV1H104J	MF 0.10UF J		
C116			C90-1456-05	NP-ELEC 0.22UF 50WV		
C117			CC45FSL1H151J	CERAMIC 150PF J		
C119			CF92FV1H472J	MF 4700PF J		
C120			C90-1331-05	NP-ELEC 0.47UF 50WV		
C121			CF92FV1H103J	MF 0.010UF J		
C122			CF92FV1H153J	MF 0.015UF J		
C123			CK45FF1H103Z	CERAMIC 0.010UF Z		
C124			CC45FSL1H470J	CERAMIC 47PF J		
C125,126			CE04KW1C330M	ELECTRO 33UF 16WV		
C127			CF92FV1H124J	MF 0.12UF J		
C128			CC45FSL1H221J	CERAMIC 220PF J		
C129			C90-1350-05	NP-ELEC 2.2UF 50WV		
C130			C90-1333-05	NP-ELEC 22UF 10WV		
C131			CF92FV1H473J	MF 0.047UF J		
C132			CF92FV1H333J	MF 0.033UF J		
C133			C90-1349-05	NP-ELEC 1UF 50WV		
C134			CF92FV1H124J	MF 0.12UF J		
C135			CK45FF1H223Z	CERAMIC 0.022UF Z		
C137			C90-1334-05	NP-ELEC 47UF 10WV		
C138			CK45FB1H102K	CERAMIC 1000PF K		
C140			CK45FF1H103Z	CERAMIC 0.010UF Z		
C142			CE04KW0J331M	ELECTRO 330UF 6.3WV		
C144			CK45FF1H473Z	CERAMIC 0.047UF Z		
C145			CE04KW1V100M	ELECTRO 10UF 35WV		
C146,147			CK45FF1H103Z	CERAMIC 0.010UF Z		
C150			CK45FB1H102K	CERAMIC 1000PF K		
C151			CE04KW1V4R7M	ELECTRO 4.7UF 35WV		
C152			CE04KW1V100M	ELECTRO 10UF 35WV		
C153			CE04KW1C330M	ELECTRO 33UF 16WV		
C154,155			CE04KW1C220M	ELECTRO 22UF 16WV		
C157			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C160			CE04KW1HR47M	ELECTRO 0.47UF 50WV		
C161,162			CE04KW0J331M	ELECTRO 330UF 6.3WV		
C163			CF92FV1H332J	MF 3300PF J		
C164			CE04KW1C330M	ELECTRO 33UF 16WV		
C165			CK45FF1H103Z	CERAMIC 0.010UF Z		
C166			CE04KW1C220M	ELECTRO 22UF 16WV		
CN1		*	E10-3502-05	FLAT CABLE CONNECTOR		
CN2			E10-1413-05	FLAT CABLE CONNECTOR		
J1	1E	*	E13-0483-05	PHONO JACK (LINE OUTPUT)		
J2	1E		E13-0131-05	PHONO JACK (DIGITAL OUTPUT)		
J3	2D		E11-0162-05	PHONE JACK (3P)PHONES		
L1 -9		*	L33-0328-05	CHOKE COIL		
L10 ,11			L40-1001-14	SMALL FIXED INDUCTOR(10UH,K)		S

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L10 ,11			L40-1001-17	SMALL FIXED INDUCTOR(10UH,K)		A
L12			L40-2292-14	SMALL FIXED INDUCTOR(2.2UH,M)		S
L12			L40-2292-17	SMALL FIXED INDUCTOR(2.2UH,M)		A
L13			L32-0328-15	OSCILATING COIL		
L14 -18			L40-2292-14	SMALL FIXED INDUCTOR(2.2UH,M)		S
L14 -18			L40-2292-17	SMALL FIXED INDUCTOR(2.2UH,M)		A
L19		*	L39-0152-05	MATCHING COIL		
L20 -23			L40-2292-14	SMALL FIXED INDUCTOR(2.2UH,M)		S
L20 -23			L40-2292-17	SMALL FIXED INDUCTOR(2.2UH,M)		A
X1			L77-1119-05	CRYSTAL RESONATOR		
R51 ,52			RN14BK2C1000F	RN 100.0 F 1/6W		
R55 ,56			RN14BK2C1003F	RN 100K F 1/6W		
R57 ,58			RN14BK2C1000F	RN 100.0 F 1/6W		
R59 ,60			RN14BK2C1961F	RN 1.96K F 1/6W		
R63 ,64			RN14BK2C9090F	RN 909.0 F 1/6W		
R65 ,66			RN14BK2C1961F	RN 1.96K F 1/6W		
R67 ,68		*	RN14BK2C1101F	RN 1.10K F 1/6W		
R69 ,70			RN14BK2C1001F	RN 1.00K F 1/6W		
R71 ,72		*	RN14BK2C1781F	RN 1.78K F 1/6W		
R73 ,74		*	RN14BK2C2611F	RN 2.61K F 1/6W		
R75 -78			RN14BK2C4641F	RN 4.64K F 1/6W		
R79 ,80		*	RN14BK2C2151F	RN 2.15K F 1/6W		
R83 ,84			RN14BK2C4641F	RN 4.64K F 1/6W		
R91 -94			RN14BK2C10R0F	RN 10.0 F 1/6W		
R110			RS14KB3D120J	FL-PROOF RS 12 J 2W		
R182			RS14KB3A100J	FL-PROOF RS 10 J 1W		
R188			RS14KB3D120J	FL-PROOF RS 12 J 2W		
R189			RS14KB3D150J	FL-PROOF RS 15 J 2W		
R213,214			RN14BK2C1001F	RN 1.00K F 1/6W		
VR1 ,2			R12-1085-05	TRIMMING POT. (2.2K)L/R LEVEL		
VR3			R12-3128-05	TRIMMING POT. (22K) TE. BAL		
VR4			R12-3126-05	TRIMMING POT. (10K) FE. BAL		
VR5			R12-1089-05	TRIMMING POT. (4.7K)FE. GAIN		
VR6			R12-3126-05	TRIMMING POT. (10K) TE. GAIN		
VR7	1E	*	R29-1001-05	POTENTIOMETER (LEVEL)		
VR8	1D		R10-4026-05	POTENTIOMETER (LEVEL)		
K1			S51-2074-05	MAGNETIC RELAY		
⚠ S1	1D		S40-1103-05	PUSH SWITCH (POWER TYPE)		
⚠ S2	1E		S31-2128-05	SLIDE SWITCH (POWER TYPE)	UMUE	
D1 -8			DSM1A1	DIODE		
D9 ,10			HZS5.1S(B2)	ZENER DIODE		
D9 ,10			RD5.1JS(B2)	ZENER DIODE		
D11			DSM1A1	DIODE		
D12			HZS8.2N(B2)	ZENER DIODE		
D12			RD8.2ES(B2)	ZENER DIODE		
D13 -18			1SS133	DIODE		
D13 -18			1SS176	DIODE		
D19			HZS13N(B2)	ZENER DIODE		
D19			RD13ES(B2)	ZENER DIODE		
D20			1SV147	VARISTOR		
D21 -28			1SS133	DIODE		
D21 -28			1SS176	DIODE		
D29			1SS131	DIODE		
D29			1SS178	DIODE		

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D30 ,31			HZS8.2N(B2)	ZENER DIODE		
D30 ,31			RD8.2ES(B2)	ZENER DIODE		
D32 ,33			HZS13N(B2)	ZENER DIODE		
D32 ,33			RD13ES(B2)	ZENER DIODE		
D34 -42			1SS133	DIODE		
D34 -42			1SS176	DIODE		
IC1			NJM4558D	IC(OP AMP X2)		
IC2 -4			M5218P	IC(OP AMP X2)		A
IC2 -4			M5218P-A	IC(OP AMP X2)		S
IC5 ,6			NJM4558D	IC(OP AMP X2)		
IC7 ,8			NJM4560D	IC(OP AMP X2)		
IC9			NJM4558D	IC(OP AMP X2)		
IC10,11			PCM56P	IC(DA CONVERTER)		
IC12			TC17G005AF-0048	IC(VCXO)		
IC13		*	CXD1088Q	IC(DIGITAL FILTER)		
IC14			CXD1125QZ	IC(DIGITAL SIGNAL PROCESSOR)		
IC15		*	CXK5816SP-12L	IC(2KX8 RAM)		
IC15		*	CXK5816SP-15L	IC(2KX8 RAM)		
IC16		*	UPD75208CW-152	IC(MICROPROCESSOR)		
IC17			CXA1081S	IC(RF AMP)		
IC18			UPD4053BC	IC(3-INPUT 2CH MPX/DE-MPX)		
IC19		*	CXA1244S	IC(SERVO SIGNAL PROCESSOR)		
IC20		*	LA6500	IC(OP AMP)		
IC22			TC74HC00P	IC(QUAD 2-INPUT NAND GATE)		
IC23			NJM4558D	IC(OP AMP X2)		
Q1			2SB772(Q,P)	TRANSISTOR		
Q2			2SD882(Q,P)	TRANSISTOR		
Q3			2SD1266(Q,P)	TRANSISTOR		
Q4			2SB941(Q,P)	TRANSISTOR		
Q5			DTC124EN	DIGITAL TRANSISTOR		
Q6			2SC3666(Y)	TRANSISTOR		
Q7			2SA1426(Y)	TRANSISTOR		
Q8			2SA1284	TRANSISTOR		
Q9			2SA733(A)(Q,P)	TRANSISTOR		
Q9			2SA999(E,F)	TRANSISTOR		
Q10			DTA124EN	DIGITAL TRANSISTOR		
Q11			DTC124EN	DIGITAL TRANSISTOR		
Q12			2SC2320(E,F)	TRANSISTOR		
Q12			2SC945(A)(Q,P)	TRANSISTOR		
Q13 ,14			2SC2878(B)	TRANSISTOR		
Q15 ,16			2SA954(L,K)	TRANSISTOR		
Q17 ,18			2SC2003(L,K)	TRANSISTOR		
Q19			2SD882(Q,P)	TRANSISTOR		
Q20			2SA1534A	TRANSISTOR		
Q21			2SA733(A)(Q,P)	TRANSISTOR		
Q21			2SA999(E,F)	TRANSISTOR		
Q22			DTC124EN	DIGITAL TRANSISTOR		
Q23			2SC2320(E,F)	TRANSISTOR		
Q23			2SC945(A)(Q,P)	TRANSISTOR		
Q24			2SA733(A)(Q,P)	TRANSISTOR		
Q24			2SA999(E,F)	TRANSISTOR		
Q25			STA341M	TRANSISTOR		
OPERATION UNIT (X25-313X-XX) 0-00: K,P,U,M,UE,X,T,E 2-71: S(T), S(E)						
D9 -14	2D		B30-1012-05	LED(SLP-981C-50)OUTPUT LEVEL		

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C1			C91-0769-05	CERAMIC 0.01UF M		
C2			CE04KW1E100M	ELECTRO 10UF 25WV		
S1 -24	2D		S40-1064-05	PUSH SWITCH		
D1 -8			1SS131	DIODE		
D1 -8			1SS178	DIODE		
FL1	2D		FIP10PM7	FLUORESCENT INDICATOR TUBE		
IC1			LB1433N	IC(LEVEL METER DRIVER)		
IC2	2D		GP-1U501	IC(REMOTE SENSOR)		
MECHANISM ASS'Y (X92-1140-01)						
C1 -3			C91-0769-05	CERAMIC 0.01UF M		
5	2B		D10-1270-14	ROD		
6	1B	*	D10-1738-04	ARM (SW)		
7	2B	*	D10-1740-03	ARM (TANGENTIAL)		
8	1B		D10-1741-13	ARM (CLAMPER)		
9	1A	*	D10-1742-02	ARM (LIFTER)		
10	2A	*	D10-1743-13	SLIDER (LIFTER)		
11	1A	*	D10-1782-24	SLIDER ASSY		
12	2A	*	D13-0359-13	GEAR (MAIN)		
13	2B	*	D13-0360-04	GEAR		
14	1B	*	D13-0361-05	GEAR ASSY (LACK)		
16	3B		D13-0363-08	GEAR		
17	2A	*	D16-0140-14	BELT		
18	3B	*	D40-0375-15	DRIVE MECHANISM ASSY		
22	1B	*	G01-1890-04	EXTENSION SPRING (SLIDER)		
23	2B	*	G01-1891-04	COMPRESSION SPRING (ARM)		
24	1B	*	G01-1892-14	COMPRESSION SPRING (ARM)		
25	1A	*	G01-1893-04	EXTENSION SPRING (TRAY ASSY)		
30	1B		J11-0086-04	CLAMPER (DISK)		
31	2B	*	J25-4976-02	PRINTED WIRING BOARD(FPC)P.U.		
32	2B	*	J91-0337-05	PICKUP		
34	1A	*	J99-0035-11	TRAY		
35	2B	*	J21-3941-14	MOUNTING HARDWARE ASSY(TRAY)		
38	2B,3B		N19-0366-04	FLAT WASHER (GEAR)		
A	1B		N09-1522-05	SET SCREW (3X8)ROD		
B	3B		N09-1814-05	TAPTITE SCREW		
E	2B	*	N09-1813-05	BAPTITE SCREW		
S1	3B	*	S46-1087-05	LEAF SWITCH (OPEN/CLOSE)		
S2	3A		S33-1019-05	LEVER SWITCH (SLT)		
43	3A	*	T42-0097-25	DC MOTOR (LOADING)		
44	3A		T42-0099-15	DC MOTOR (DISK)		
45	2A	*	T42-0100-04	MOTOR ASSY		

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DP-880SG

SPECIFICATIONS

[Format]

Type: ..... Compact disc player
Read system: ..... Non-contact optical pickup
Laser: ..... GaAlAs, wave-length=780nm, 3-beam tracking
Rotational speed: ..... About 500 to 200 rpm
Error correction: ..... Cross Interleave Read-Solomon code
Audio channels: 2

[Audio]

Frequency response: ..... 4Hz ~ 20kHz
Signal-to-noise ratio: ..... more than 100dB
Total harmonic distortion: ... 0.003% at 1kHz
Channel separation: ..... more than 100dB at 1kHz
Wow flutter: ..... Below measurable limit
Output voltage
Analog outputs
LINE OUT (FIXED): 2.0V
LINE OUT (VARIABLE): .... 0 ~ 2.0V
Digital output
Coax cable terminal: ..... 0.5V p-p, 75 ohms
Headphone jack: ..... 60mW (8 ohms)

[General]

Power consumption: 23W
Dimensions: ..... W: 440mm ($17\frac{5}{16}$")
H: 104mm ($4\frac{1}{8}$")
D: 313mm ($12\frac{5}{16}$")
Weight: 5.4kg (11.9lb)

[Wireless remote control unit]

Model: RC-P880SG
Type: ..... Infrared pulse
Power supply: ..... DC 3V (two AA size batteries)
Weight: ..... 115g (with batteries)

[Supplied accessories]

Connection cord: ..... 1 stereo cord
Wireless remote control (RC-P880SG): 1
Batteries (AA): 2

Note:
We follow a policy of continuous development.
For this reason specifications may be changed without notice.

Note:
Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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